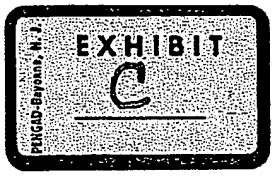

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ABSTRACT

This document describes the Phased Array Communication Antenna System (PACAS). PACAS receives direct broadcast satellite (DBS) television and other signals from orbiting satellites via a fuselage-mounted, electronically steered, phased-array antenna, and provides the signal to a compatible receiver. The intended use of the system is on commercial, private, or military airplanes having a video distribution and display system and/or the ability to receive and decode other high-speed data streams through the antenna system.

KEY WORDS

Airplane
Antenna
Direct-Broadcast
Phased Array
Receiver
Satellite
Television

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ACRONYMS AND ABBREVIATIONS

A	Amperes
AC	Alternating current
A/D	Analog-to-digital
ARINC	Aeronautical Radio, Incorporated
ASIC	Application-specific integrated circuit
ASU	Antenna switch unit
AWG	American Wire Gauge
BITE	Built-in-test equipment
BSS	Broadcast Satellite Service
CMOS	Complementary metal-oxide silicon
CONUS	Continental United States
COTS	Commercial-off-the-shelf
CPU	Central-processor unit
dB	Decibels
DBS	Direct broadcast satellite
DC	Direct current
DSS	Digital Satellite Service®
EBSC	External beam-steering controller
EEPROM	Electrically erasable programmable read-only memory
EPLD	Erasable programmable logic device
FCC	Federal Communications Commission
FSS	Fixed Satellite Service
GHz	Gigahertz
GND	Ground
IF	Intermediate frequency
IFE	In-flight entertainment
IR	Infrared
IRU	Inertial reference unit
LHCP	Left-hand circular polarization
LNA	Low-noise amplifier
LNB	Low-noise block, down converter
LRU	Line-replaceable unit
mA	Milliamperes
MHz	Megahertz
MMIC	Monolithic, microwave integrated circuit
NOVRAM	Non-volatile, random-access memory
OT	Overtemperature
PS	Power Supply
PACAS	Phased-Array Communication Antenna System
QUICC	Quad-integrated communications controller
PDC	Processor/data calculator card
PLD	Programmable logic device
PWB	Printed wiring board
RAM	Random-access memory
RF	Radio Frequency
RHCP	Right-hand circular polarization

RSU	Receiver switch unit
RX or RXD	Receive data
SPAC	System Phased Array Controller
SRU	Shop-replaceable unit
STARS	Satellite TV airborne receiving system
TBD	To be determined
TPWB	Teflon printed wiring board
TTD	True-time delay
TV	Television
TX or TXD	Transmit data
UHF	Ultra-high frequency
UL	Underwriters Laboratories
USSB	United States Satellite Broadcasting
V	Volts
WAIM	Wide-angle impedance matching

1. SCOPE

1.1 Identification

This document describes the phased-array communication antenna system (PACAS, formerly satellite TV airborne receiving system, or STARS).

1.2 System Overview

The purpose of the phased-array communication antenna system (PACAS) is to provide direct broadcast television and data reception capability for commercial and private planes for passenger entertainment and airline revenue.

1.3 Document Overview

This document provides a description of the operations and capabilities of the phased-array communication antenna system. Detailed system and line-replaceable unit (LRU) requirements are documented in the PACAS Requirements Document (D909-80003).

Section 3 describes the system architecture and operations. Section 4 describes the LRU designs and operations.

2. REFERENCE DOCUMENTS

The following documents are applicable to the design and operations of the phased array communication antenna system.

2.1 Government

MIL-STD-1472D	Human Engineering Design Criteria for Military Systems, Equipment, and Facilities, 14 March 1989.

2.2 Industry

ARINC 429	Mark 33 Digital Information Transfer System (DITS), July 1980
ARINC 485	Cabin Management and Entertainment System, Part 1, Head End Equipment Protocol (Draft 3, dated July 21, 1997).
EIA-232	Standard Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange

2.3 Boeing

D909-80003	PACAS Requirements Document
D909-80006	PACAS Hardware Interface Control Document
D909-80018	PACAS BITE Coverage Analysis

D909-80026 PACAS Software Requirements Document

D909-80054 Hardware/Software Interface Document

STARS-CKTS-CONT-002 STARS Phased Array Controller Baseline, STARS Project Note, Revision New, 10-23-95.

STARS-SW-CONT-007 Users Guide for Special Purpose Test Software (SPTS) for the Phased Array Systems Organization (PASO) Dual Polarity Receiver Controller Software, STARS Project Note, Revision A, 31 July 1997.

STARS-SY-CONT-008 STARS Tracking Algorithm Description and Analysis, STARS Project Note, Revision A, January 15, 1996.

STARS-SY-CONT-009 True Time Delay Algorithms and Optimization, STARS Project Note, Revision Draft New, December 27, 1995.

STARS-PKG-CABL-023 Drawing Tree for Phased Array Systems Interconnect Cabling, STARS Project Note, Revision New, 7/22/97.

STARS-SY-CONT-131 Phase Only Computations for True Time Delay Control, STARS Project Note, Revision New, 10/16/97.

2.4 Thomson Consumer Electronics

DSS-1 Integrated Receiver/Decoder Product Specification for Wideband/Low Speed Ports, version 3.2, (draft) 19 November 1996.

2.5 EchoStar Corporation

6996 Serial Interface for Peripheral Control, Version 1.0, June 18, 1996. Revision dated August 7, 1996.

3. SYSTEM DESCRIPTION

3.1 Definition and Configurations

The phased array communication antenna system (PACAS) provides direct broadcast television reception capability for commercial, private, and military airplanes for purposes of passenger entertainment and airline revenue. It is designed to provide this entertainment on the ground or during cruise conditions (limited roll and pitch angles) over the continental United States (CONUS), and will also provide continuous service (including landings and takeoffs) at airports serving the southern United States.

Although it may be used worldwide for the DBS band (11.7 to 12.7 GHz), the performance of the system is based on operation over CONUS. PACAS is designed to receive signals from the Hughes DBS satellites located at 101°W longitude in geosynchronous orbit (equatorial latitude), and from the DISH Network (EchoStar) satellites located at 119°W longitude. Other receivers can be substituted to obtain signals from other satellites as they become available, providing worldwide coverage.

In addition, PACAS can be configured to receive user data from fixed satellite service (FSS) satellites or equivalent in the Ku-band (11.7-12.7 GHz). System performance and data rate depend on the satellite selection, ground station, and airplane interfaces.

The PACAS receive system receives a DBS signal, converts the frequency, and outputs the RF to satellite-compatible receivers. For the wide-band (true-time delay) option, the number of television channels is limited only by the DBS signal and the receiver capability (the narrow-band (non-TTD) option has a bandwidth limit of approximately 110 MHz). PACAS provides the DBS signals to the receivers concurrently on two dedicated RF outputs, which reflect the two input polarizations from the satellites (left-hand circular polarization (LHCP) and right-hand circular polarization (RHCP)).

The PACAS data function can receive signals from satellites and convert them to serial data streams on the airplane. These can be used for such applications as video teleconferencing, transfer of data files, and real-time network access (*e.g.*, Internet). These are potential applications not yet implemented in the baseline described herein.

The PACAS context is depicted in figure 3.1-1. In addition to the DBS signal, PACAS also receives ARINC 429 position and attitude information, which speeds the acquisition of the DBS signal but is not required for operation. PACAS provides a visual indication of operational and fault status on one of its line-replaceable units (LRUs), and also makes the status available via an external status interface.

The interface to the receiver is defined to be compatible with existing home DBS receivers. Because of the proprietary nature of the encoded DBS signal, the receiver is required to provide confirmation to PACAS that it has acquired signal from the correct satellite (*i.e.*, a satellite for the correct service provider with the correct programming).

PACAS uses one 115V AC, 400 Hz, 3-phase input to provide power for the receive antenna function, and either multiple 115V AC 60 Hz or 400 Hz inputs for the COTS receivers or receiver switch units, respectively. Airplane mounting provisions are customized for a particular

airframe and may be further tailored for specific airline customers. The phased-array antenna provides a low-drag configuration, due to its low profile on the top of the fuselage. The balance of equipment is installed near the antenna location but within the fuselage. The PACAS controller can be remotely located near the external receiver, if desired.

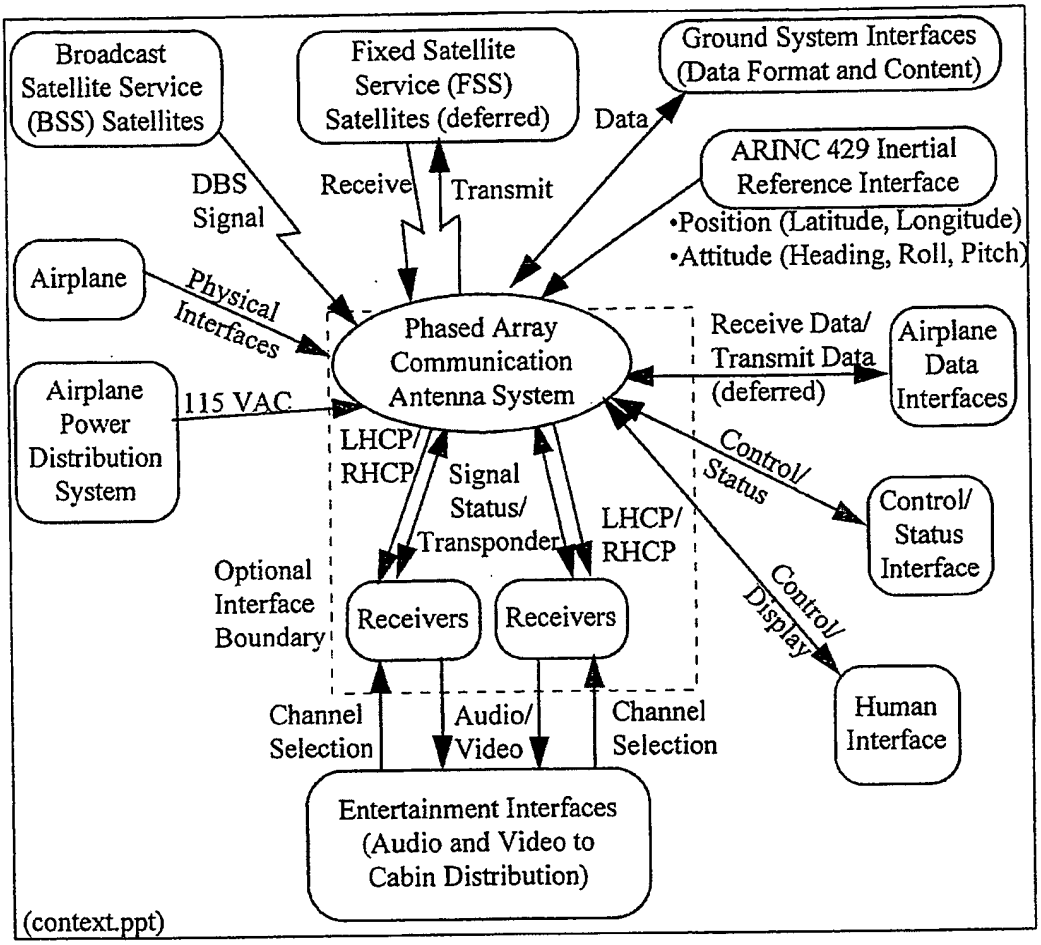


FIGURE 3.1-1. PACAS CONTEXT DIAGRAM

PACAS is designed for flexibility in the configuration of receivers/decoders while maintaining a stable "core" of four LRUs (antenna, controller, power supply, LNB) which bring the satellite signal to the receivers. The receiver configuration can be tailored from two basic options: (1) antenna switch unit (ASU) plus commercial-off-the-shelf (COTS) receivers (1 to 24, figure 3.1-2), or (2) receiver switch unit (RSU), which integrates the functions of the (ASU) and COTS receivers (figure 3.1-3).

TABLE 3-1. PACAS LRUS

LRU	Functions
Receive Antenna	Receive radiated 11.7 to 12.7 GHz DBS signal in right-hand circular and left-hand circular polarizations (concurrently), and convert to two, Ku-band conducted outputs as either 11.7-12.2 or 12.2-12.7 GHz.
LNB	Convert 500 MHz of input Ku-band, 11.7-12.2 or 12.2-12.7 GHz DBS signal into 0.95 to 1.45 GHz signal for each of two polarizations.
System Phased-Array Controller (SPAC)	Provide phasing/steering commands to antenna; control LNB band selection; receive/process/report/display system operational and fault status; interface with receivers and external interfaces for system operations.
Power Supply	Provide all system DC power. Monitor and control antenna power for over-temperature and fault conditions. Provide status to controller.
Antenna Switch Unit	Multiplex RHCP and LHCP inputs to 12 COTS receivers; provide RS-232 signal validation mapping to selected receiver. Supports up to 24 receivers (2 ASUs).
Receivers (COTS)	Decode DBS signal into audio and baseband NTSC video.
Receiver Switch Unit	Provides same functionality as and replaces [ASU + COTS Receivers]. Provides up to 24 channels audio/video (multiple units). Also provides high-speed serial data (100 Mbps).
Cables	Provide interconnections between LRUs.

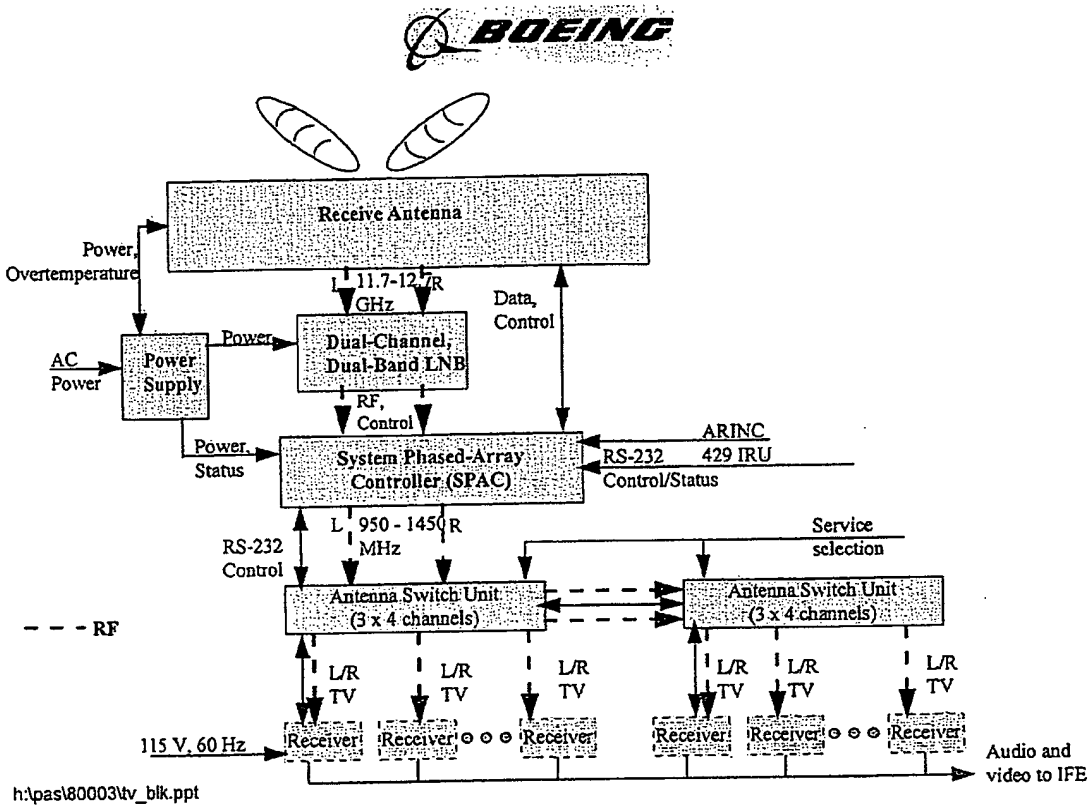


FIGURE 3.1-2. PACAS BLOCK DIAGRAM (ASU CONFIGURATION)

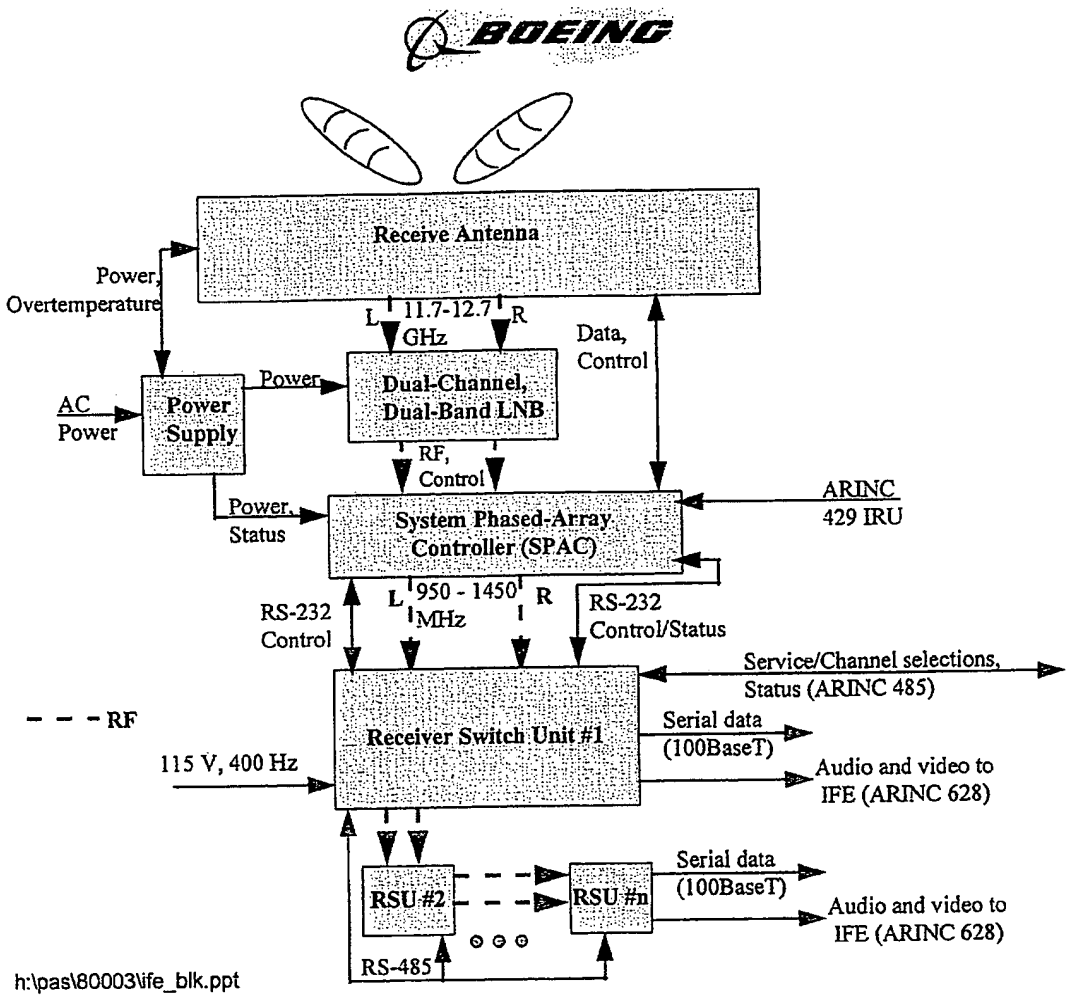


FIGURE 3.1-3. PACAS BLOCK DIAGRAM (RSU CONFIGURATION)

3.2 Core System Operations

The PACAS top-level functional flow is indicated in figure 3.2-1. PACAS is intended to operate without any operator intervention. There is, therefore, no "control panel" required for the core system.

PACAS operates in two states: "acquire" and "maintain" (or "track") satellite signal. Status reporting and power interrupt handling are background tasks independent of operational state.

Upon application of power, PACAS searches the sky for a source or RF power, beginning with the last known position stored in memory. When one is successfully acquired (the receiver indicates that it successfully decodes the signal), PACAS changes to the "track" state and follows the apparent motion of the satellite as the plane position, attitude and heading change. Status reporting includes a two-digit status code displayed on the PACAS controller (SPAC, System Phased Array Controller), and which is also transmitted on an optional external maintenance interface. The monitoring and test concept links intrusive testing to loss of function, which reduces the probability of nuisance faults (faults which are reported with no associated

loss of function). Upon loss of power, PACAS retains the last known satellite position for use in re-acquiring the DBS signal.

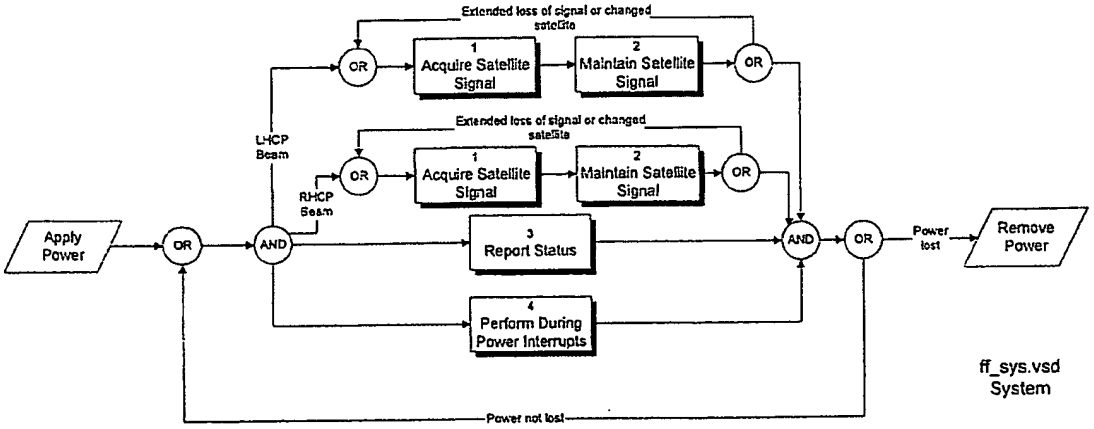


FIGURE 3.2-1. PACAS FUNCTIONAL FLOW

3.2.1 Initialization and Acquire State

Upon application of power PACAS immediately begins the process of acquiring a DBS signal for each of the two polarizations; there is no separate "initialization" state (figure 3.2-2). If available, the retained position and tuning band (frequency) are initially used (two tuning bands are available: the "North America" DBS band (12.2-12.7 GHz) for broadcast television (also called, Broadcast Satellite Services, or BSS), and the Fixed Satellite Service (FSS) band from 11.7-12.2 GHz. PACAS begins searching the sky at the last known position, or, if none is available, by going through a catalog of known satellite locations, based on the present position (determined from the ARINC 429 inertial reference unit input). These include the Hughes DBS-1, -2, and -3 satellites at 101.1° W longitude, and the EchoStar-1 and -2 satellites at 119° W longitude (additional satellites are being added on a regular basis: TEMPO2 is on-orbit at 119° W longitude (though not fully functional); EchoStar-3 is on-orbit at 61.5° W longitude and EchoStar-4 is on-orbit and moving toward its final location at 145° W longitude are also on-orbit (data as of 7/98)). If no sources are found at expected locations, PACAS begins searching the whole sky for RF sources. During this portion of the process the SPAC will display a code indicating that it has not yet detected an RF source (codes 92, 93, 94 depending on detection of RF from either or neither beam).

During this time the SPAC also attempts to establish communication with each of two receivers, one for each polarization, via the LHCP and RHCP RS-232 receiver ports. If the SPAC establishes communication with exactly one receiver (either EchoStar type or DSS type), the SPAC changes operation to a "beam slaving" mode, wherein both LHCP and RHCP beams are managed to ensure that they continually point to the same satellite constellation.

When PACAS has found a source of in-band RF energy, the signal is provided to the external receiver, and PACAS requests validation from the receiver using a Signal Status Request on the receiver databus (beginning with the Thomson communications protocol, followed by the EchoStar communications protocol if there is no response to the Thomson protocol). The receiver returns Signal Status Response as either "good signal" or "bad signal". If the signal is

"good", PACAS changes to the "track" state. If the signal is "bad" PACAS continuously scans the sky and provides each available RF source to the receiver for validation. If no response is received from the receiver, PACAS continuously points and tracks RF power at the last known location. In beam slaving mode, response from one receiver validates both polarization beams.

After providing all possible sources in the upper tuning band (12.2-12.7 GHz) without receiving signal validation, PACAS switches the LNB to the lower band (11.7-12.2 GHz), and the process is repeated. PACAS remains in the acquire state until it receives "good signal" from the receiver.

If the system is commanded into "open-loop track" via the control/status interface, PACAS will point the applicable beam(s) to the commanded geostationary longitude, and maintain absolute pointing regardless of feedback from the receiver. This function is implemented without regard to received RF power, and may not be as accurate as closed-loop tracking to the same location. Therefore, it is recommended that it be used only when closed-loop tracking is not available (insufficient RF power or no receiver feedback available). An alternate method to track on RF power without receiver feedback is to place the system into Engineering Mode (see section 3.3.4.2) and command either or both beams to "track".

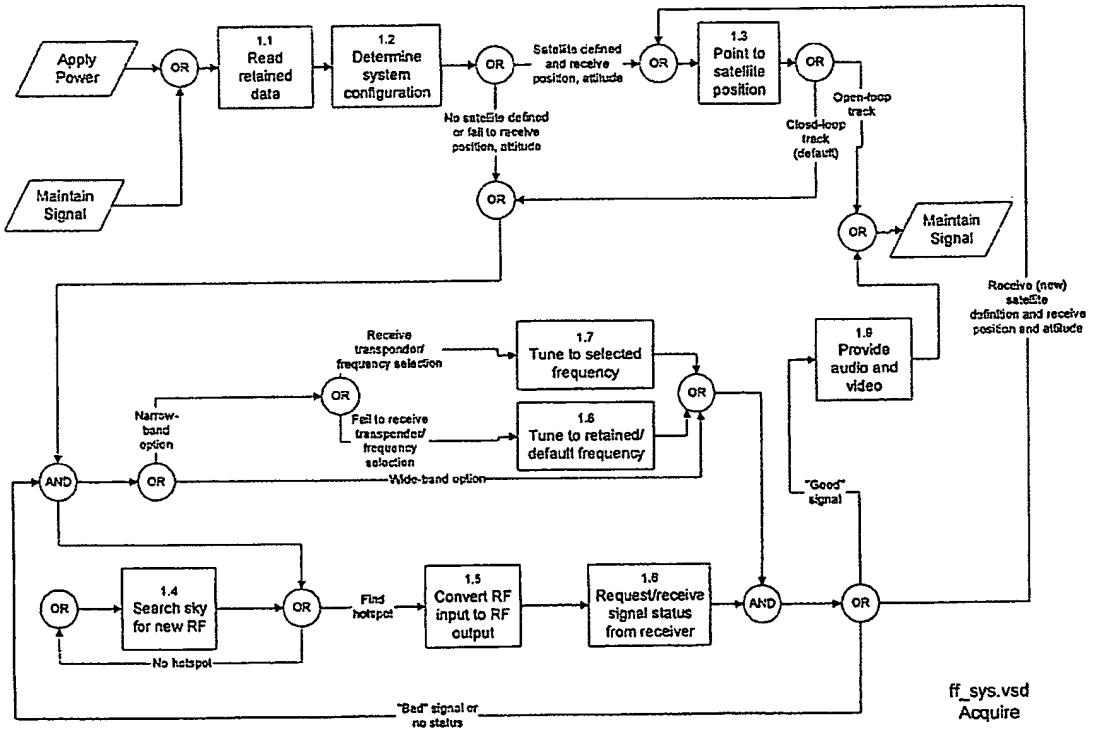


FIGURE 3.2-2. ACQUIRE STATE FUNCTIONAL FLOW

3.2.2 Track State and Normal Operation

During the track state (the normal operational condition, figure 3.2-3) PACAS maintains the DBS signal to the receiver. The SPAC causes the antenna to continuously steer the beam at and around the known satellite location in order to follow any apparent changes in relative position.

As the beam pointing is modified, PACAS determines the RF energy at each point, and recalculates the new, most probable satellite location (see SPAC description in section 4.4).

The bandwidth of the SPAC-antenna steering and control loop allows the PACAS to maintain DBS output through airplane maneuvers up to 6°/second of roll/pitch/yaw.

If, during the track state, PACAS loses the DBS signal (RF energy drops below minimum), PACAS maintains beam pointing at the last known satellite position (through any subsequent maneuvers) for 1 minute. This feature allows PACAS to quickly recover the DBS signal after temporary loss of signal due to an obstruction or heavy clouds or precipitation.

One minute after loss of signal, or if the receiver continuously indicates a "bad signal", PACAS reinitiates the acquire state and again searches for a valid DBS signal.

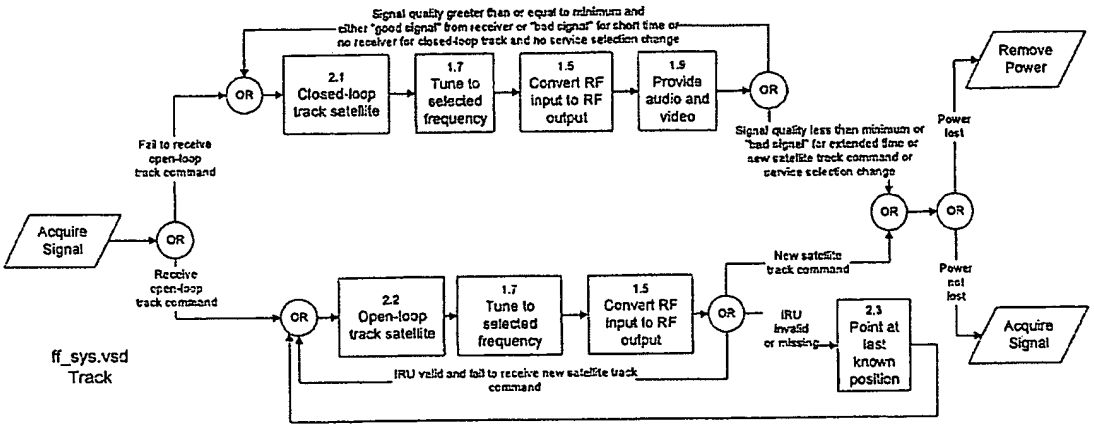


FIGURE 3.2-3. TRACK STATE FUNCTIONAL FLOW

3.2.3 Status Reporting

The functional flow for status reporting is displayed in figure 3.2-4. The monitoring system is composed of two key system-level operational monitors (RF output to the receiver and signal status from the receiver), plus additional "internal status" monitors to perform fault detection and isolation.

All failures will be "latched" (retained through power interrupts) to help resolve intermittent faults, and must therefore be "unlatchable". PACAS implements the "unlatch" function using a SPAC-based switch. Faults (including operational status) are displayed on the SPAC, and reported via the control/status interface for remote display. The control/status interface also supports fault unlatching and operational control.

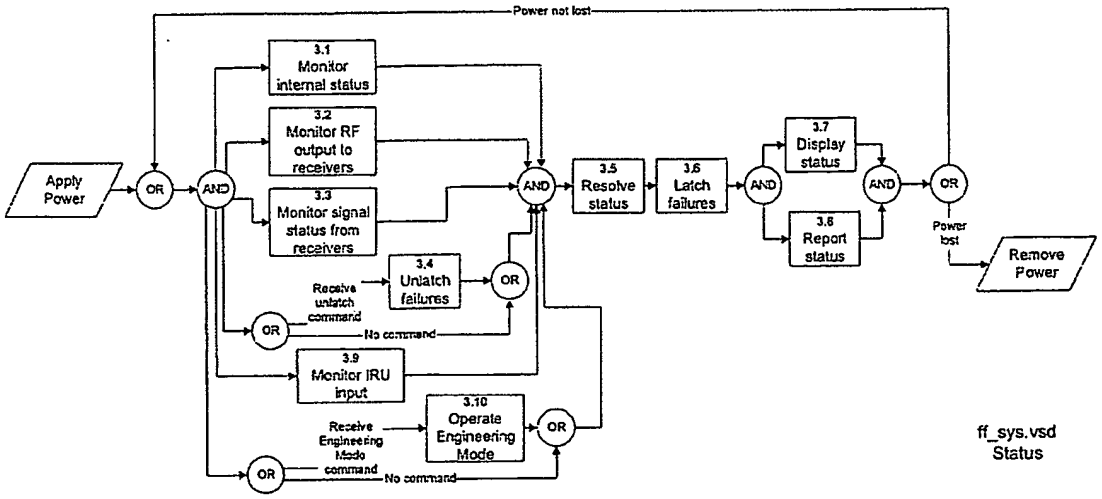


FIGURE 3.2-4. STATUS REPORTING FUNCTIONAL FLOW

The philosophy of the fault detection/isolation/reporting system is to detect faults through observables. That is, PACAS will be evaluated for maintenance only after a passenger, crew, or maintenance person determines that there is a loss of DBS function and the maintenance person wishes to isolate the fault and make repairs. The requirements for fault detection are therefore couched in terms of detecting enough faults that PACAS can isolate the faults to a single LRU, and requiring that only "functional" faults (those that cause loss of DBS output) be detected and isolated.

This approach reduces the perception of "nuisance faults" (indications of failure which cannot be related to a system loss of function), because PACAS will only monitor or test functions in the absence of DBS function. The "down-side" is that failures of the monitoring provisions themselves become "latent" faults, which may result in incorrect isolation in the presence of a subsequent loss of function.

For example, failure of a power supply status monitor to the SPAC will be ignored until there is a loss of DBS. At that time the SPAC will attempt to isolate the failure which produces the loss of DBS and will detect a "power supply" fault due to the monitor alarming, even if the loss of DBS is due to the absence of input signal.

However, this situation is unavoidable unless monitors or tests are added to verify that the monitors themselves are functioning correctly (so called, "BITEing the BITE"). The BITE Coverage Analysis (D909-80018) documents that the relative failure rates of monitors compared with the functions being monitored is less than 10% of the system failure rate, so that the occurrences of monitoring faults are relatively rare.

The absence of monitoring individual functions except in the presence of detected loss of function allows the system to eliminate a "self-test" operating mode as a high-level function, thus eliminating the need to externally control the system operational states. Without operator intervention, the SPAC will automatically initiate intrusive tests to perform fault isolation whenever there is a loss of DBS function, even while continuing to attempt to acquire a satellite signal.

3.2.4 Power Interrupt Handling

Because of the high power requirements of the antenna, any loss of input power causes the antenna to immediately lose RF output to the LNB and SPAC (the alternative is holdup capacitors in the power supply, with size dependent on the holdup time). This causes loss of DBS signal to the receiver, which results in an immediate "freeze frame" of the video picture from the receiver, followed by the receiver entering its "waiting for input" mode.

Because of this sequence and the expense of holding up power, PACAS has been designed only to retain antenna pointing information during a loss of power (any length that causes the power supply to disable its outputs, figure 3.2-5). This pointing information allows PACAS to quickly recover the satellite location and output following restoration of power.

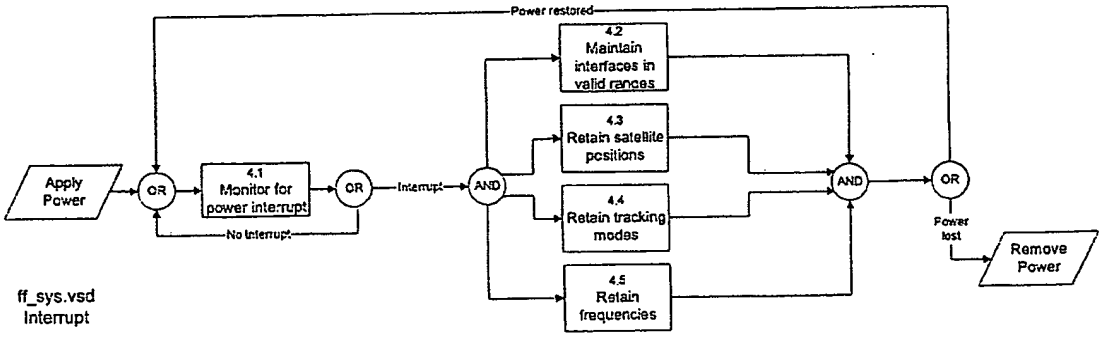


FIGURE 3.2-5. POWER INTERRUPT FUNCTIONAL FLOW

3.3 Inter-LRU Operation

PACAS inter-LRU functions are identified on the system block diagrams (figures 3.1-2 and 3.1-3) and in the list of PACAS LRUs, table 3-1.

3.3.1 System Power

The power supply provides all power from the airplane to the other three core LRUs (receivers are powered separately) (figures 3.1-2, 3.1-3). When provided with 115V AC power, the power supply automatically turns on 19.5V DC power to the SPAC and LNB. The power supply checks the antenna for an overtemperature condition, then turns on power to the antenna in the absence of an overtemperature indication. The complete functional flow for the power supply is indicated in figure 3.3-1.

While providing power, the power supply continuously monitors for input power interrupts, antenna overtemperature, and faults in its output interfaces. When a SPAC power fault is detected, all power (antenna and SPAC) is inhibited, and the fault condition is latched until input power is cycled.

When an antenna power fault is detected, -5 and +6/+5 power to the antenna is inhibited, status is provided to the SPAC, and the fault condition is latched until input power is cycled. When an antenna overtemperature condition is detected, power to the antenna is inhibited only until the overtemperature condition is removed, whereupon antenna power is resupplied automatically.

When an input power interrupt is detected, the power supply limits its outputs to not exceed the maximum allowables during shut down. When power is restored, all latched fault conditions are cleared and the power supply begins operation as above.

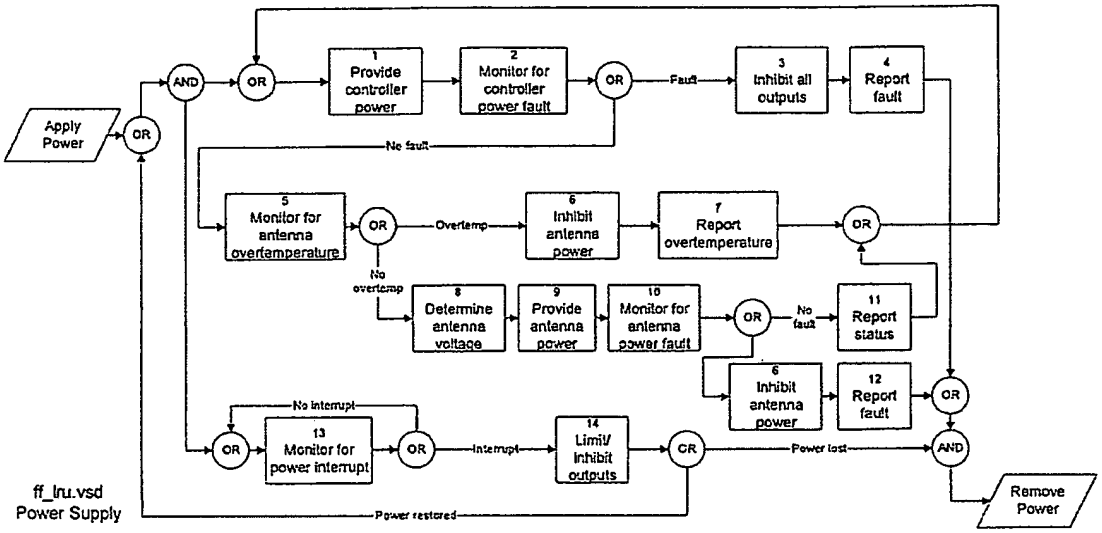


FIGURE 3.3-1. POWER SUPPLY FUNCTIONAL FLOW

3.3.2 RF Operations

As seen in figures 3.1-2 and 3.1-3, Ku-band RF illuminates the antenna, which converts it to conducted Ku-band RF under control of the SPAC (which steers the beam and selects the band and frequency of operation). Within the antenna the outputs of individual antenna elements (1515 "modules") are phased and combined into the two polarization outputs. In the wide-band option, outputs from each of the six subarrays (groups of 256 modules) are delayed in time with respect to each other (so-called, true time delay, or TTD), to ensure the same beam pointing for all frequencies within the required 500 MHz bandwidth (in the narrow-band option, the absence of the TTD limits the instantaneous bandwidth to approximately 110 MHz). The antenna functional flow is indicated in figure 3.3-2.

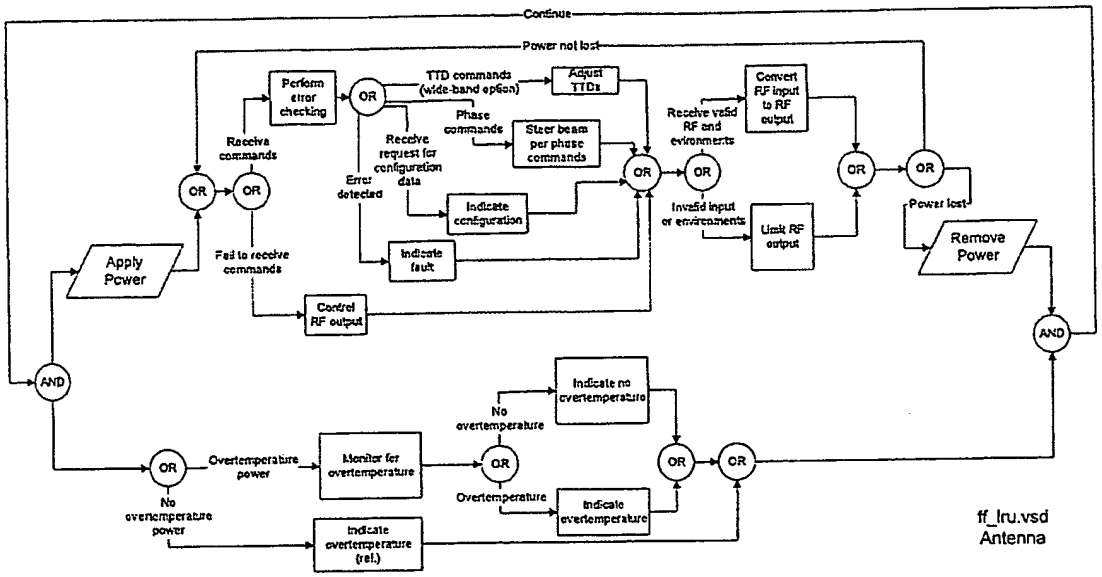


FIGURE 3.3-2. ANTENNA FUNCTIONAL FLOW

For each of the two polarizations the conducted RF is delivered on a 2-to-4-foot cable to the low noise block/down converter (LNB), where the signal is downconverted and amplified into an intermediate frequency (IF) of 950-1450 MHz. Band selection within the LNB from the antenna input is under control of the SPAC, using a DC level on the IF coaxial cable between the LNB and SPAC, independently for each of the two polarizations. The LNB functional flow is indicated in figure 3.3-3.

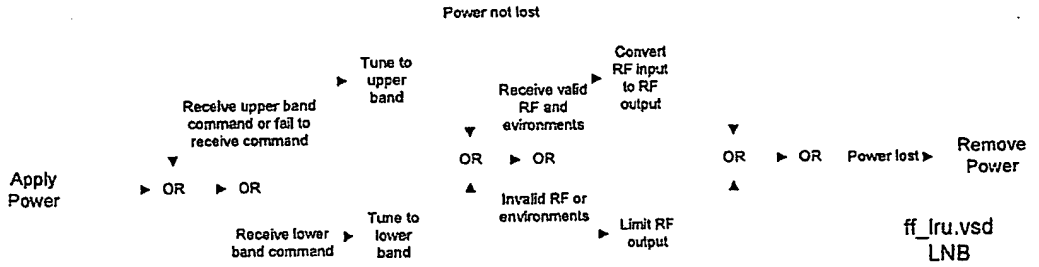


FIGURE 3.3-3. LNB FUNCTIONAL FLOW

In the SPAC, the input RF for each polarization is split, with half going out to downstream receiver(s), and half to the internal RF detector (section 4.4.3), which continuously measures the RF power, providing feedback to the SPAC processor for each position of the beam (section 3.3.3).

In open-loop tracking, SPAC simply points the selected polarization(s) to the requested location, and maintains pointing through airplane changes in attitude and position (*i.e.*, the RF power measurement may be unused). This operational mode requires the use of an inertial reference unit (IRU) to indicate to the SPAC the airplane attitude and position.

From the SPAC, the RF is delivered to one or more receivers (see receiver operations below) for conversion to audio/video or other data streams.

3.3.3 Pointing, Tracking and True Time Delay

In addition to the closed-loop tracking process (rather than only pointing in response to input from an IRU, "open-loop tracking"), one other key performance feature of PACAS is obtaining high instantaneous bandwidth (500 MHz) using a true-time delay (TTD). These two features give PACAS performance advantages in wide-band communications for mobile platforms compared with competing technologies.

3.3.3.1 Beam Pointing

The SPAC computes a 4-bit phase shifter setting for each element of the 1536 antenna elements. The antenna is divided into 512 element sections with each section sub-divided into two 256 element sub-arrays (each sub-array actually includes only 505 active elements because of the need for through-bolts and other structural considerations). The phase shifter settings are computed from the operating frequency and the pointing angles θ (scan angle) and ϕ (azimuth angle). The angles θ and ϕ are shown in figure 3.3-4, where X is the direction of forward airplane motion.

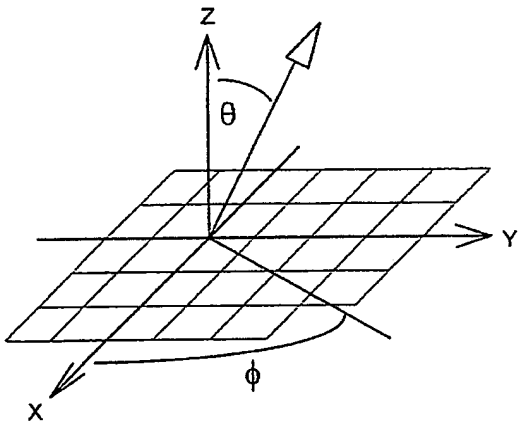


FIGURE 3.3-4. SCAN AND AZIMUTH ANGLE GEOMETRY

The angles θ and ϕ are converted to setup parameters for the data calculation hardware. The data calculator hardware (in the SPAC, section 4.4.2) then computes the phase shifter settings. The setup parameters are computed as follows:

First compute the phase differences in the x and y directions.

$$\delta_y = \frac{360 \cdot \nu \cdot \Delta_y}{c} \sin\theta \sin\phi \qquad \delta_x = \frac{360 \cdot \nu \cdot \Delta_x}{c} \sin\theta \cos\phi$$

where:

ν = operating frequency (11.7 to 12.7 GHz)
θ = beam angle from zenith (0 to 90 degrees)
ϕ = azimuth beam angle (0 to 360 degrees)

c = speed of light
Δ_x = grid spacing in the 'x' direction
Δ_y = grid spacing in the 'y' direction

Next compute the initial, delta, and flyback phase values that will be sent to the data calculator hardware (reference figure 3.3-5).

$$\text{phaseI}_{00} = -\gamma - 22.5 \cdot \delta_x - 15.5 \cdot \delta_y$$
$$\text{phaseI}_{01} = \text{phaseI}_{00} + 16 \cdot \delta_y$$
$$\text{phaseI}_{10} = \text{phaseI}_{00} + 15 \cdot \delta_x + \gamma$$
$$\text{phaseI}_{11} = \text{phaseI}_{10} + 16 \cdot \delta_y$$
$$\text{phaseI}_{20} = \text{phaseI}_{10} + 15 \cdot \delta_x + \gamma$$
$$\text{phaseI}_{21} = \text{phaseI}_{20} + 16 \cdot \delta_y$$
$$\text{phaseD} = \delta_y$$
$$\text{phaseF}_0 = -\delta_x - 15.5\delta_y$$
$$\text{phaseF}_1 = -\delta_x - 14.5\delta_y$$

The initial phase values (phase I_{mn}) correspond to the lower left element of each of the six 256 element sub-arrays. The delta phase value (phase D) is the difference between two elements along a clock line. The two flyback values (phase F_n) are used to jump from the 16th data row to the 1st row of the next clock line. Two flyback values are used to account for the element stagger between adjacent columns (see diagram below).

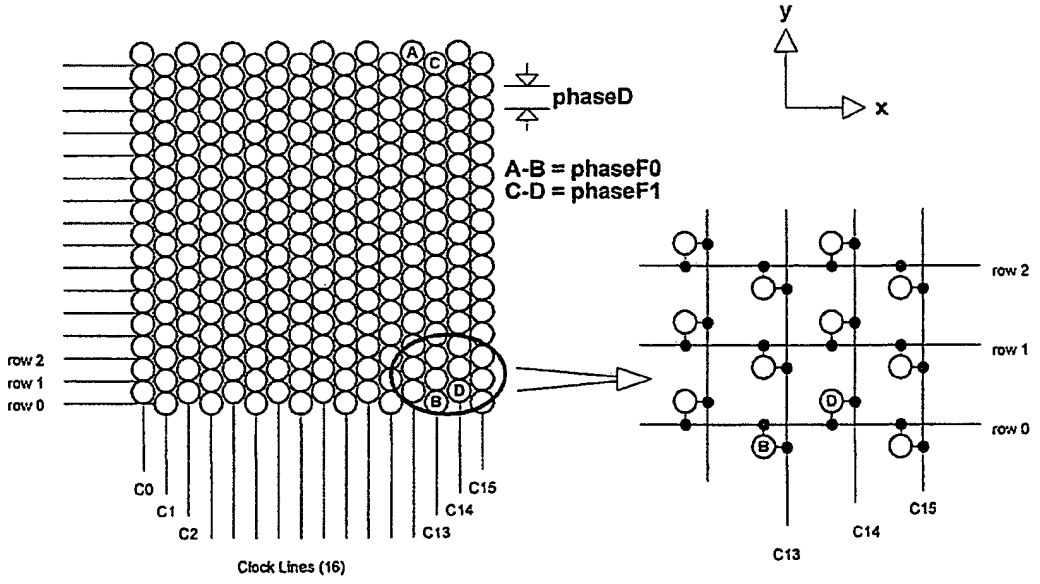


FIGURE 3.3-5. SUB-ARRAY GEOMETRY

3.3.3.2 Tracking Algorithm

To track the location of the DBS satellite with respect to the PACAS antenna a conical scan is used (reference STARS-SY-CONT-008, figure 3.3-6). In each 10-millisecond cycle, the SPAC steers the beam around the current center point, evaluating RF power at each location (a technique known as, "sequential lobing"). The SPAC then computes a new "center" position of highest power based on interpolation of the five points measured, and the cycle repeats. This process is applied independently for each beam while in closed-loop tracking mode. This mode of operation (closed-loop tracking on RF power) gives PACAS its unique capability to (1) track independently of IRU input, (2) track at very low RF power levels, and (3) track at high rates of angular change.

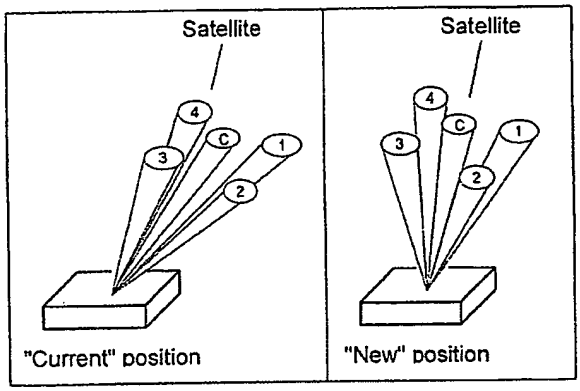


FIGURE 3.3-6. SEQUENTIAL LOBING PROCESS

The beam of the antenna is intentionally pointed away from the expected satellite location by a known amount and the signal strength is estimated. By pointing the beam at a variety of angles around the estimated satellite position (forming a cone), the estimated satellite location is updated. This is done independently for each beam in closed-loop tracking mode (even during beam-slaving operation to a single receiver, the tracking of each beam is independent of the other so long as they remain with 1° of each other).

For the operational conditions we have established (offsets of 0.3 dB, SNR of 5.0 dB, integration times of 1.25 ms), the tracking algorithm degrades the performance by less than an additional 0.04 dB (1-σ). (The analysis only treats the idealized thermal noise statistics and not other sources of received signal fluctuation.)

The antenna is assumed to consist of an approximately rectangular array of closely spaced elements, not necessarily on a rectangular grid, with axes-lengths L_x and L_y. We represent the true satellite direction vector by (u_{xs}, u_{ys}), and, the estimated position by $(\hat{u}_{xs}, \hat{u}_{ys})$. The values are the estimated projected wavenumbers of the satellite direction on the x- and y-axes. In our spherical coordinate system $(R, \hat{\theta}_s, \hat{\phi}_s)$, where $\hat{\theta}_s$ is measured from the +z axis, and $\hat{\phi}_s$ is measured from the +x-axis (positive toward the y-axis) this implies

$$\hat{u}_{xs} = 2\pi L_x \sin(\hat{\theta}_s)\cos(\hat{\phi}_s)/\lambda$$

$$\hat{u}_{ys} = 2\pi L_y \sin(\hat{\theta}_s)\,\sin(\hat{\phi}_s)/\lambda.$$

For an arbitrary pointing direction, (u_x, u_y), we can approximate the gain on the satellite by:

$$G(u_{xs} - u_x, u_{ys} - u_y) = G_0[\sin(\delta_{ux}/2)/(\delta_{ux}/2)]^2[\sin(\delta_{uy}/2)/(\delta_{uy}/2)]^2$$

where: $\delta_{ux} = (u_{xs} - u_x)$ and $\delta_{uy} = (u_{ys} - u_y)$. This ignores the impact of the embedded element gain, but for large arrays this is small.

For our method of sequential lobing we intentionally offset the beam in phase-space and point it at 5 positions, 4 around the periphery and one in the center. Ideally, all 4 on the periphery receive an identical power, less than the 5th position by a prescribed amount. We can determine an offset δ_u such that

$$G(\delta_u, 0) = G(0, \delta_u) = \rho G_0.$$

A very accurate approximation obtained from a Taylor expansion is:

$$\delta_u = 2\sqrt{10 - \sqrt{100 - 120 * \left[1 - \sqrt{\rho}\right]}}\;; \quad \text{for } 0.5<\rho<1.0.$$

Note that δ_u is independent of scan angle or axis. However, the geometric angle shift is dependent on scan angle and is larger for larger scan angles. Table 3.3-1 lists some typical values.

TABLE 3.3-1. SCAN OFFSET VS. TRACKING POWER

Power Ratio ρ (dB)	Power Ratio ρ (linear)	δ_u, radians
-0.1	0.97724	0.52505
-0.2	0.95499	0.74168
-0.3	0.93325	0.90733
-0.5	0.89125	1.16870
-1.0	0.79433	1.64353
-2.0	0.63096	2.29898
-3.0	0.50119	2.78613

The 5 beam positions and associated measured powers then become: $(\hat{u}_{xs}, \hat{u}_{ys})$

$$\mathbf{u}_0 = (\hat{u}_{xs} - \delta_u,\ \hat{u}_{ys}),\ \hat{P}_0$$
$$\mathbf{u}_1 = (\hat{u}_{xs} + \delta_u,\ \hat{u}_{ys}),\ \hat{P}_1$$
$$\mathbf{u}_2 = (\hat{u}_{xs},\ \hat{u}_{ys} - \delta_u),\ \hat{P}_2$$
$$\mathbf{u}_3 = (\hat{u}_{xs},\ \hat{u}_{ys} + \delta_u),\ \hat{P}_3$$
$$\mathbf{u}_4 = (\hat{u}_{xs},\ \hat{u}_{ys}),\ \hat{P}_4$$

Each component, u_r, must be limited to $2\pi L_r/\lambda$, or it would imply a scan angle outside of visible space. For an element at position (x_i,y_i) in the array, with (0,0) being the centroid, the relative phase shift setting is given by:

$$\theta_{ps}(x_i,y_i) = x_i\, u_x/L_x + y_i\, u_y/L_y \quad \text{(in radians)}$$

After 5 beam positions are computed, an update of the satellite position estimate is made by performing a quadratic fit:

$$\hat{u}'_{xs} = \hat{u}_{xs} + \tfrac{1}{2}\delta_u \frac{\hat{P}_1 - \hat{P}_0}{2\hat{P}_4 - \hat{P}_1 - \hat{P}_0}$$

$$\hat{u}'_{ys} = \hat{u}_{ys} + \tfrac{1}{2}\delta_u \frac{\hat{P}_3 - \hat{P}_2}{2\hat{P}_4 - \hat{P}_3 - \hat{P}_2}$$

Clearly, the denominator should not be 0, which would be indicative of a straight line, nor should it be negative, indicative of a concave data set. We further limit the adjustment to no more than one of the interval endpoints, *i.e.*, extrapolations are not allowed.

A timeline for the tracking algorithm is shown below. The process starts with hand-off from acquisition. The acquisition algorithm passes the angles θ and ϕ to the tracking algorithm. The tracking algorithm computes the setup parameters for the data calculator and commands it to compute phase shifter settings for the right hand beam (**Cmd_1R**). The data calculator loads the phase shifters while the tracking algorithm computes the setup parameters for the left hand beam. Every 675 μsec, the data calculator sends phase shift data to the antenna. Data is alternated between the right and left hand beams. At 1.35 msec intervals the phase shift data is latched into the antenna when the data calculator sends a latch command (**Latch-n**). This process continues with the tracking algorithm reading the RF measurements at the points shown in the timeline. Once all five readings are made, the tracking algorithm computes a new position for the satellite (thus updating the angles θ and ϕ) and starts the cycle over again. A total of 7, 1.35-millisecond states are used in the tracking algorithm. Five states are used to perform the sequential lobing while the additional states are used to update TTD settings and perform other computations. This continues until either the SPAC is commanded to stop or the algorithm loses track of the satellite, in which case the SPAC will reenter the acquisition phase. The algorithm takes 9.45 msec to update the satellite position given a nominal 1.35 msec beam pointing update period.

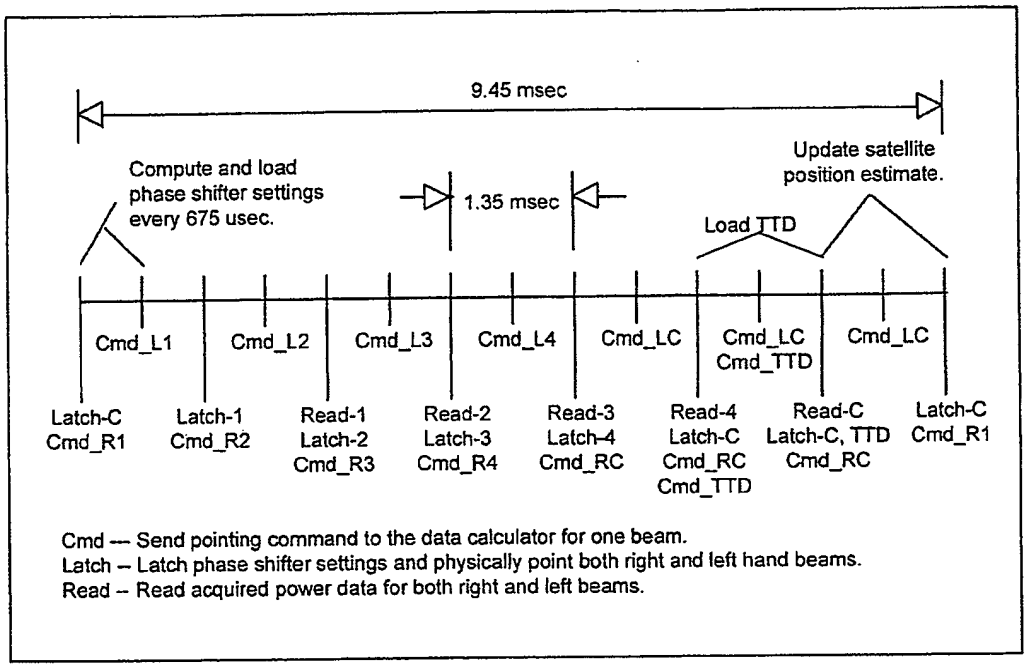


FIGURE 3.3-7. TRACKING ALGORITHM TIMELINE

3.3.3.3 True Time Delay

The true-time delay (TTD) elements of the system (SPAC, EBSC, and TTD) enable the antenna to provide an instantaneous bandwidth of about 500 MHz (compared with about 110 MHz without the TTD), by converting the effective aperture size (as regards beam squint) to that of a single sub-array of 256 elements (approximately 8" square). Invocation of the TTD causes the sub-array outputs to be combined after passing through temporal delay-lines, whose lengths are selected in the SPAC based on calculations of scan angle and azimuth. The delay lines in the antenna TTDs are switched using low-loss PIN diodes.

Insertion of a temporal delay implements a portion of the phase difference between array elements as a time delay applicable to all frequencies, rather than a phase delay which is accurate at only one frequency. The remaining phase difference between elements must still be implemented using the phase shifters in the modules. Quantization of the TTD delay lines also requires that some portion of the calculated temporal delay between adjacent subarrays be allocated (added) to the phase calculation.

3.3.3.3.1 Delay Calculation (reference STARS-SY-CONT-009)

TTD delay lines are quantized (only discrete values are available). A value of 1.9" equivalent free space delay (τ=161 ps) is used as the minimum delay. Therefore, a value of 1τ is the minimum quantized delay that can be inserted between subarrays (equivalent to a scan angle $\theta=\sin^{-1}(1.9"/8")=14°$). At a scan angle of 70°, a delay of 4τ (=(8"/1.9")sin(70°)) is required between adjacent subarrays along the satellite azimuth, or a total of 8τ between two subarrays.

Section 4.1 contains the antenna RF circuit block diagram, including the TTDs (figures 4.1-2 and 4.1-12, a total of 12 TTDs (1 per subarray per polarization)). Each subarray may be delayed by one of 9 possible time delays before being combined with other subarrays along the x-axis. The central subarrays have the highest resolution which we call the TTD least significant bit, represented by "τ". The TTD provides delay lines of 1τ, 2τ, 3τ, and 6τ, which may be combined in two stages to produce relative delays of 0τ through 8τ, in 1τ increments. The exterior subarrays have the capacity for setting the delay in steps approximately double this resolution. There is a further capability of an additional delay between the two halves of the antenna in the y-axis of 0τ or 1τ. This implies that the 4 exterior subarrays have a resolution of approximately 2τ, while the central subarrays have a resolution of τ. Table 3.3-2 indicates the array geometry.

TABLE 3.3-2. ARRAY DIMENSIONS (REFERENCE FIGURE 3.3-5)

Between elements (Triangular grid) (inches)	Between Subarrays (inches)	Overall Array Length (inches)
$D_x = 0.454$	$S_x = 16*D_x + 0.736$ $= 8.000$	$L_x = (2*S_x+16*D_x)$ $= 23.264$
$D_y = 0.524$	$S_y = 16*D_y$ $= 8.384$	$L_y = (2*S_y)$; $= 16.768$

The other important figure of merit is the maximum error over the bandwidth of interest due to quantization. This can be computed by: $\varepsilon_{max} = \pm 2\pi(B/2)(\tau/2)$ (=0.126 radians = 7.2°) for the central subarrays and twice this for the 4 corner subarrays.

A requirement for uncertainty in phase of approximately 5° would require knowing the TTD delay to approximately 1 picosecond. This is almost impossible to design for. If the accuracy is reasonably good, say 50 picoseconds, $\tau \approx 0.161$ ns, then the error in delay can be removed at any one frequency with a phase shift compensation derived from a calibration of the combiner circuit. This is accomplished by updating the array element compensation tables.

The antenna retains the insertion phase of the TTD at the mid-band frequency for each arm at each possible setting. The SPAC then compensates for the insertion phase errors of each subarray due to the quantization at any specified scan angle at this mid-band frequency by allocating the phase difference remaining after insertion of the TTD delay to the phase shifters, assuming the mid-band frequency (11.95 GHz or 12.45 GHz). A beam skew loss comes about because of the wide bandwidth, B, of the system and the inaccuracy of the time delays due to quantization.

In each tracking period (10 ms) the SPAC calculates the new beam-pointing position, determines the TTD settings (next section), allocates "residual phase" to the phase shifters, and begins the cycle anew.

3.3.3.3.2 TTD Update Rate (reference STARS-SY-CONT-131)

The TTD settings are revised whenever a change in the propagation time between adjacent subarrays exceeds some minimum value. This "minimum value" would be the inserted time delay between adjacent subarrays that most closely represented the actual time delay, given that

the delay values are quantized. The TTD can be controlled using phase only. This is possible because the antenna is tuned exclusively to the mid-band frequency. In the BSS band this is 12.45 GHz. At that frequency the time delay can be converted to a phase shift and applied directly to the beam steering calculations.

The initial phase value for each subarray is adjusted by subtracting out the amount of phase that is being inserted by the TTD circuits. The inserted phase has two terms, the first being the design value of the TTD and the second a calibration constant that is determined in the manufacturing test process. The initial phase is computed as:

$$I_\phi = N_x \cdot dx + N_y \cdot dy - TTD_\phi + TTD_{cal}$$

where dx and dy are the inter-element phase differences in the x and y directions and N_x and N_y are the distances, in module spacing, from the center of the active antenna area to the first element of a given subarray. This calculation, less the TTD parts, is already done as part of the normal beam steering function of the controller.

$$\delta_x = \frac{360 \cdot \nu \cdot \Delta_x}{c} \sin\theta \cos\phi$$

$$\delta_y = \frac{360 \cdot \nu \cdot \Delta_y}{c} \sin\theta \sin\phi$$

The TTD phase value is computed by multiplying the desired TTD setting by ϕ_τ, which is the designed phase value for a single setting.

$$TTD_\phi = N_\tau \cdot \phi_\tau$$

The TTD setting is computed from the phase numbers, dx and dy, and the per step TTD phase. The simplest approach is just to round off the computation and use the resulting integer N_τ. Rounding in this case means the usual adding or subtracting 0.5 depending on the sign of the argument and then truncating the result.

$$N_\tau = round\left(\frac{N_x \cdot \delta_x + N_y \cdot \delta_y}{\phi_\tau}\right)$$

However, to prevent oscillating between TTD settings, hysteresis is built into the TTD control algorithm.

$$N_{th} = round\left(\frac{N_x \cdot \delta_x + N_y \cdot \delta_y}{\phi_\tau} - hysteresis\right)$$

$$N_{tl} = round\left(\frac{N_x \cdot \delta_x + N_y \cdot \delta_y}{\phi_\tau} + hysteresis\right)$$

Given the two integers N_{th} and N_{tl} the desired TTD setting is determined from the following pseudocode:

```
1.  if (Nth > Ntl)
2.          Nτ = Nth;          -- Above hysteresis, set higher setting
3.  else if (Nth == Ntl)
```

4. $N_\tau = N_{tl}$; -- Below hysteresis, set lower setting
5. else if ($N_\tau == N_{th}$ OR $N_\tau == N_{tl}$)
6. $N_\tau = N_\tau$; -- Current setting is valid so keep it.
7. else if ($N_{tl} < 0$) -- Made a large jump in beam position
8. $N_\tau = N_{tl}$; -- Desired setting is the low one.
9. else if ($N_{tl} > 0$)
10. $N_\tau = N_{th}$; -- Desired setting is the high one.
11. else
12. $N_\tau = 0$; -- Desired setting is zero.
13. end

Lines 1-4 compare the high and low values. If the high value is greater then use it. If the two are equal then use the lower number. If neither case fits then we're in the hysteresis region and need to keep the current value of N_τ, but we only want to keep it if it is valid. The only time it would be invalid is if we made a large change in beam position (but this can't happen because extrapolations are not allowed). Lines 7-12 select a setting based on the sign of the computed value of the lower number. This logic is performed for each subarray.

We want to change the TTD setting by the minimum of 1τ whenever such a change would improve the system performance. This is accomplished using the algorithm described above. Figure 3.3-8 shows the minimum scan angle change vs. scan angle that will cause a change in the TTD setting. At a roll/pitch/turn rate of 6 degrees/second, the maximum update rate for changes in the TTD would be once every 2 seconds. Equivalently, at constant θ a change in ϕ causes an update to the TTD setting at the same maximum rate.

The SPAC checks the TTD adjustment criterion every tracking frame (every 10 ms). The TTD is adjusted only if the adjustment criterion is satisfied. Therefore, the TTD is capable of being updated by the SPAC every 10 ms (every tracking frame), but, in practice, would not be expected to be adjusted any faster than every few seconds under the most dynamic conditions (6°/second). The adjustment criterion defined above suggests that the TTD should never need to be changed by more than 1τ at a time in any direction ($\pm 1\tau$ in -x or in -y).

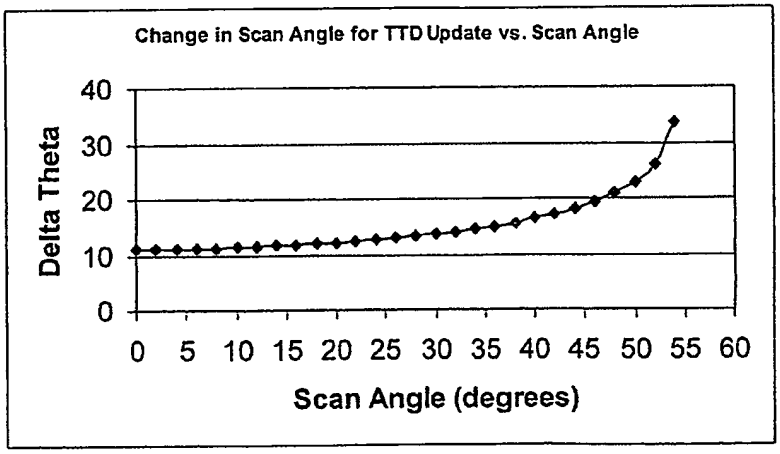


FIGURE 3.3-8. SCAN ANGLE CHANGE FOR TTD UPDATE VS. SCAN ANGLE

When a TTD delay is inserted, the delay line provides a phase delay equivalent to the inserted delay divided by the center frequency of the operating band (either 11.95 or 12.45 for lower and upper bands, respectively).

Summary. To implement TTD control, in each tracking cycle the SPAC (1) retains θ and ϕ from the last TTD adjustment, (2) compares them to θ and ϕ for the new beam center in the current tracking cycle, (3) adjusts the TTD settings if triggered by the criteria, and (4) adjusts the phase shifter values to compensate for that portion of phase difference allocated to the TTD (considering the insertion phase compensation for the current TTD setting).

3.3.4 System Control

3.3.4.1 Normal Operation

System control is distributed between the power supply and the SPAC (figure 3.3-9). Upon receiving power, the SPAC first checks for a change in the antenna configuration information, and downloads new data from the read-only memories in the antenna (from the external beam-steering controllers, EBSC) if the data has changed. The SPAC then begins commanding the antenna to point to the last known satellite position(s), based on retained data and input from the inertial reference unit. The SPAC also commands the LNB to the last known tuning band (upper, at 12.2-12.7 GHz, or lower, at 11.7-12.2 GHz).

The power supply controls power to the antenna, LNB, and SPAC, monitoring for adverse conditions, and also inhibits power to the antenna when the antenna indicates an overtemperature condition (reference figure 3.3-2). Status is continuously provided to the SPAC for processing, reporting, and display.

When the SPAC begins receiving measurable RF power from the antenna and LNB, the SPAC queries the receiver(s) for signal quality. The receivers indicate their ability to decode the signal. If the SPAC fails to receive "good signal" from the receiver, it stays in the "acquire" state and continuously searches for an RF signal which satisfies the receiver (figures 3.3-9 and 3.3-10).

When the receiver indicates "good signal" the SPAC transitions to the track state and tracks the RF power source.

The SPAC receives frequency selection from the receiver (narrow-band option only, as a result of channel selections). The RS-232 Control/Status interface to the SPAC provides mode-control (open-loop vs. closed-loop tracking, and Engineering Mode), satellite selection (initial location for closed-loop tracking), and frequency control, and reports PACAS status up to the ASU/receiver interfaces.

The ARINC 429 interface from the inertial reference unit (IRU) provides airplane attitude and position. This information is optional for closed-loop tracking, wherein it reduces initial acquisition time. It is generally unused during tracking except for total loss of signal. IRU input is required for open-loop tracking (PACAS will not perform open-loop tracking without an IRU).

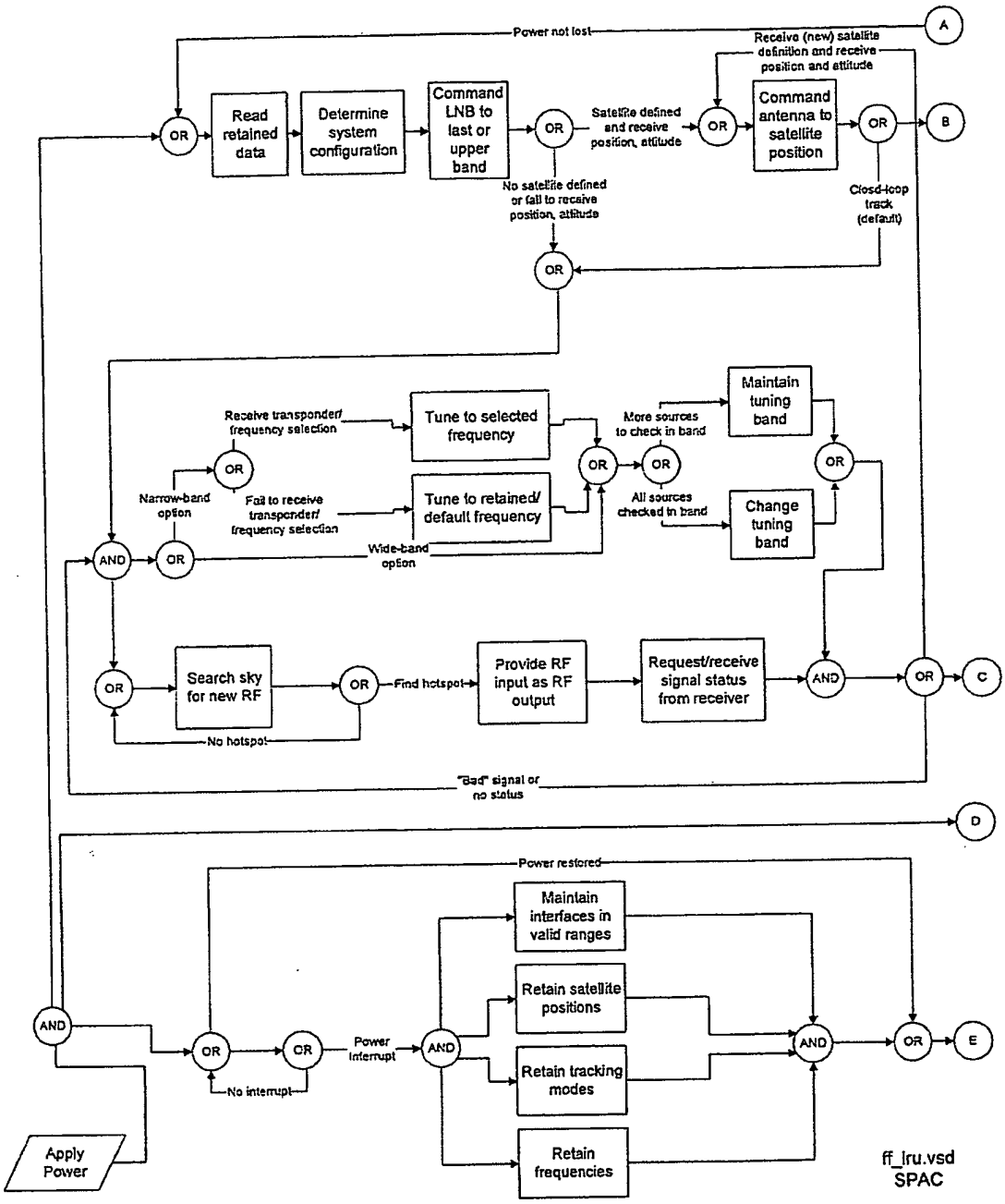


FIGURE 3.3-9. CONTROLLER FUNCTIONAL FLOW (1 OF 2)

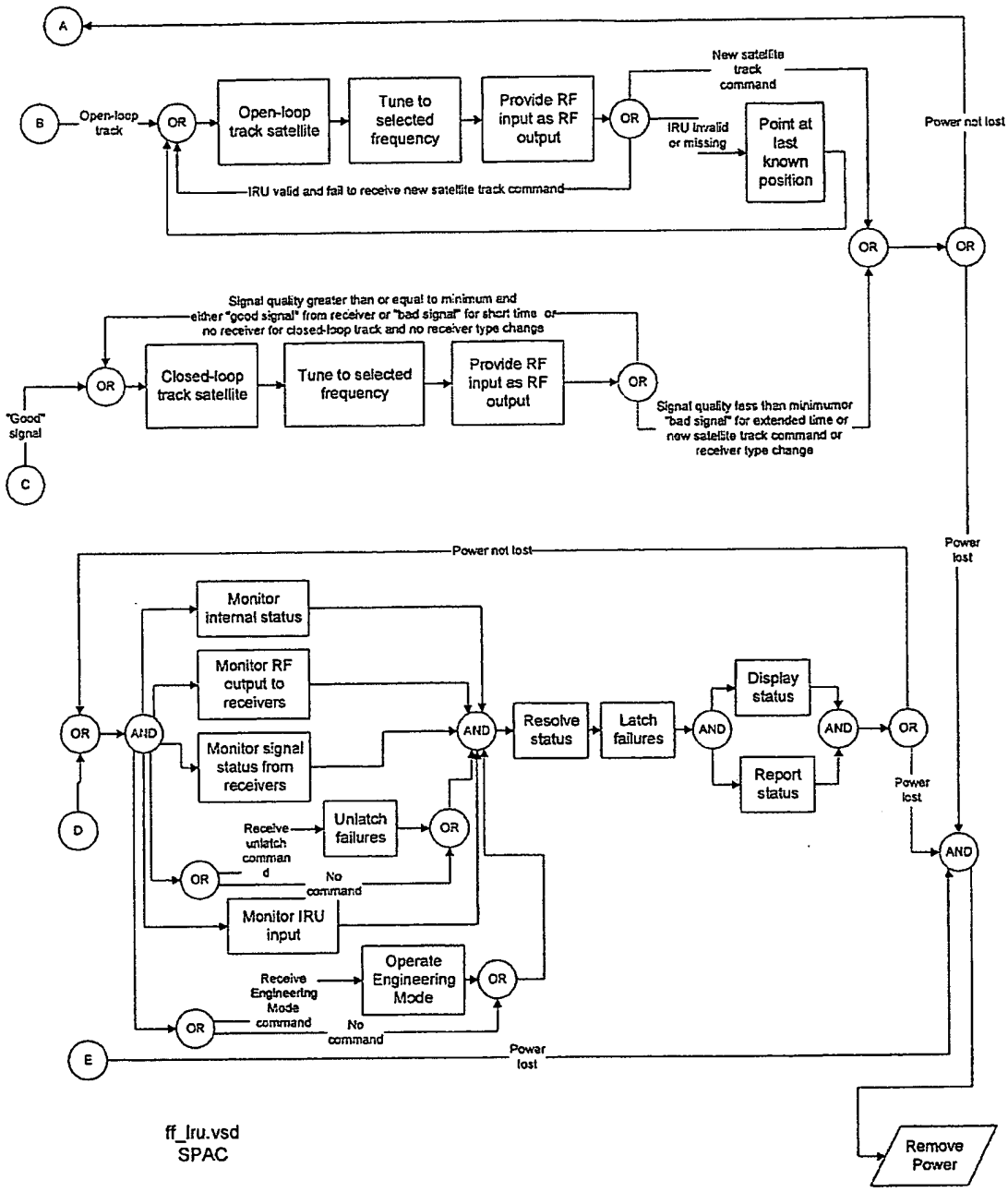


FIGURE 3.3-10. CONTROLLER FUNCTIONAL FLOW (2 OF 2)

3.3.4.2 Engineering Mode

Engineering Mode provides the capability to (a) command the system into operational and non-operational states, and (b) obtain detailed information regarding the status of the system and associated external equipment. Mode capabilities have been defined to support (a) antenna performance testing, (b) system integration, checkout, and performance verification, and (c) system performance monitoring during operations. Although designed to be executed

concurrently with other system operations, maximum tracking rates may be degraded because of the additional processor loads on the SPAC. Periodic fault status on the Control/Status interface is suspended during Engineering Mode (the data still is available on command).

The complete list of commands and functions is listed in the SRD table 3.2.3.5-2. The functions are executed via the SPAC RS-232 Control/Status interface using ASCII characters (reference STARS-SW-CONT-007). A "Windows 95" application has been prepared for executing all functionality of the Control/Status interface, including Engineering Mode.

3.3.5 Receiver Operations

As discussed in 3.2, two receiver configurations are baselined: (1) COTS receivers in conjunction with an ASU, and (2) RSUs. These configurations allow one or more passengers to select and view independent television channels. A third configuration, where one or two receivers are directly connected to the SPAC LHCP or RHCP ports (RF and RS-232 Signal Validation), are considered to be a singular case of the ASU configuration (without the ASU and polarization selection functions). The receiver then talks directly to the SPAC; a channel change to the unsupported polarization causes loss of output.

All receivers must be "authorized" by the service provider (*e.g.*, EchoStar or DirecTV) to decode and output selected programs. The industry approach requires that every receiver contain a separate "access card" which contains a decoder "key". When a program (*e.g.*, Cable News Network) becomes authorized for a receiver, the service provider transmits an authorization which is received by the antenna and receiver as part of the incoming data from the satellite. The receiver decodes the data, compares the authorization content for its own serial number and the serial number of its access card, and then retains the authorization which enables the receiver to decode the applicable program. Such authorizations have a limited lifetime (of order 1-2 months), and are updated regularly and automatically by the service provider.

3.3.5.1 ASU/COTS Receiver Operations

The use of COTS receivers brings the home environment to the mobile platform. Channel selection is made in the receiver using on-screen selections controlled by the user via an ultra-high-frequency (UHF) or infrared (IR) remote, or using the receiver front panel (figure 3.3-11).

When a channel is selected, the receiver outputs a DC level to the ASU via the RF input cable to select the polarization applicable to the selected channel. At the same time, the receiver tunes to the satellite transponder which contains the requested channel, and decodes and outputs the selected program (video and audio outputs to television).

For the receivers which are on ASU ports 1, 5, or 9, exactly one is selectable at any time (via an external ground discrete into the ASU) for communication with the SPAC. This selected receiver validates the RF signal as discussed above, selecting the satellite location which is consistent with its decoding type (DSS or digital video broadcast (DVB)). For narrow-band antennas, the receiver also indicates the selected transponder frequency to the SPAC in conjunction with its channel selection.

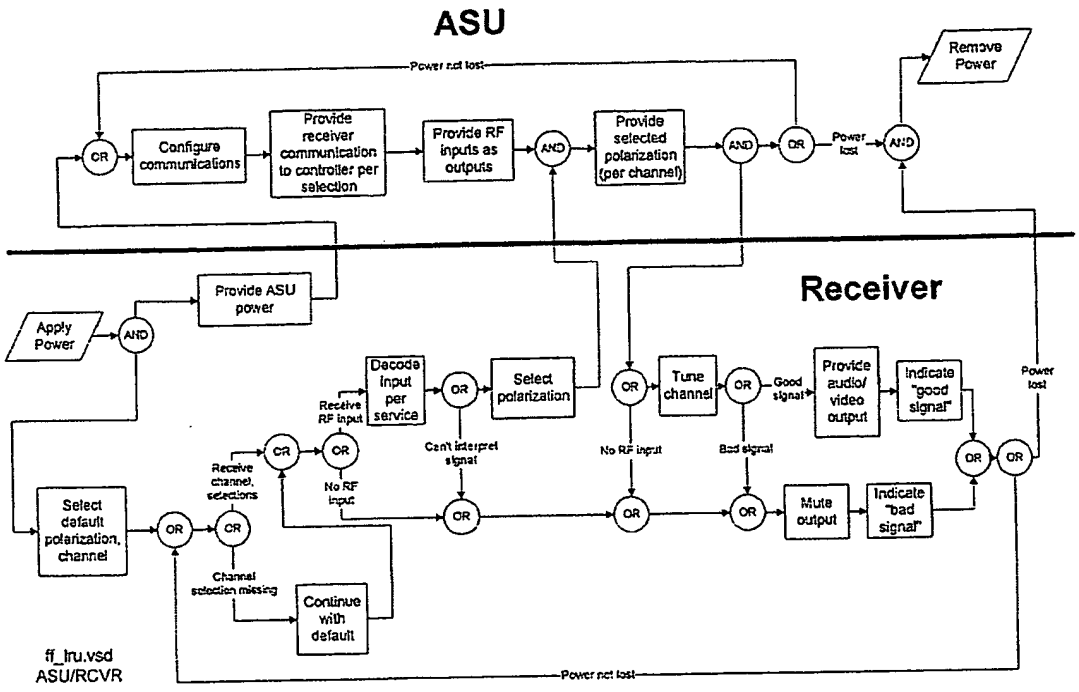


FIGURE 3.3-11. RECEIVER FUNCTIONAL FLOW (ASU CONFIGURATION)

3.3.5.2 RSU Operation

[The RSU baseline configuration is controlled by Aviation Information Services rather than Phased Array Systems. The following brief description is included only for completeness. The RSU configuration assumes an additional control panel connected to RSU#1 via an ARINC 485 standard bus.]

The RSU provides (1) multiple channels of television service from a single package, (2) a single interface point for the SPAC for signal validation, frequency control, and operational control and status, and (3) a control point for ARINC 485-standard operation and status to/from an external controller, such as a control panel (figure 3.3-12). The RSU also performs fault consolidation and processing for the core LRUs and each of the RSUs. RSU requirements are captured in TBD.

The initial RSU configuration supports 4 channels of television; 24 channels are achieved by cascading 6 RSUs. Inter-RSU control and status is via an additional RS-485 bus (figure 3.1-3).

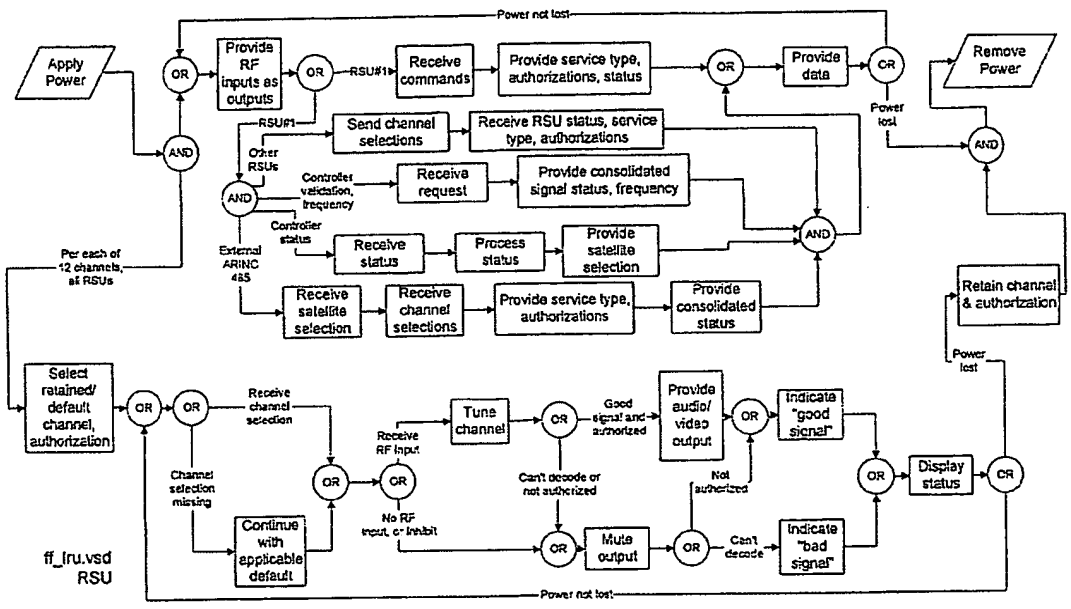


FIGURE 3.3-12. RECEIVER FUNCTIONAL FLOW (RSU CONFIGURATION)

3.4 Monitoring and Test Concepts

The basic philosophy of fault monitoring and operational testing (*aka*, built-in-test, or BIT/BITE) is to:

- Allocate primary fault monitoring to the user, based on the audio and video outputs.
- Limit fault isolation activity to operate in response to a detected loss of function.
- Limit fault isolation to only that necessary to isolate on-airplane with high confidence (90% to a single or most-probable LRU).

These three ground rules result in a greatly simplified BITE design which relies primarily on operational monitors already available in the system. Limiting fault isolation to operate only in response to a detected loss of function reduces the quantity of nuisance faults attributable to failures of the BITE monitors.

The digital nature of the encoded TV signal makes the approach of reporting faults only for loss of function more easily achievable. The receiver "downstream" of the PACAS SPAC indicates when the digital "bit-error rate" (BER) exceeds a threshold above which it is unable to convert the DBS signal (or equivalently, the signal-to-noise ratio falls below the minimum required value). Under this condition the receiver "mutes" its output (temporary "freeze" of picture, then indicates "looking for satellite"), and indicates to the SPAC that it has a "bad signal" (polled status from SPAC). Concurrently, the SPAC may measure that the RF power has dropped below its minimum threshold. Therefore, loss of function as detected by the receiver may also be discerned as a loss of function by the SPAC (SPAC can detect and track on power levels that may be insufficient for the receiver to decode; therefore, loss of function detected by the receiver (inability to decode) may not be detected concurrently by the SPAC (loss of RF power)). The

SPAC attempts to isolate faults using the status it receives from other LRUs and by conducting intrusive tests.

Except for faults of the ARINC 429 and Control/Status interfaces and any BITE, all other faults of PACAS are related to the ability of PACAS to provide DBS to the receiver and receiving validation thereof (and loss of the ARINC 429 input *may* cause loss of DBS if PACAS is unable to acquire or maintain tracking in its absence). Because PACAS fault monitoring and test provisions are limited to operating primarily when PACAS determines that it is providing invalid DBS signal to the receiver, the likelihood of nuisance faults is reduced, and the SPAC expends a very small amount of its throughput performing BITE.

The following sections describe the BITE concepts for each of the major functional areas: Power, Electronics, and RF.

3.4.1 Power

Figure 3.4-1 indicates the operational and fault monitoring (BITE) features of the PACAS power system.

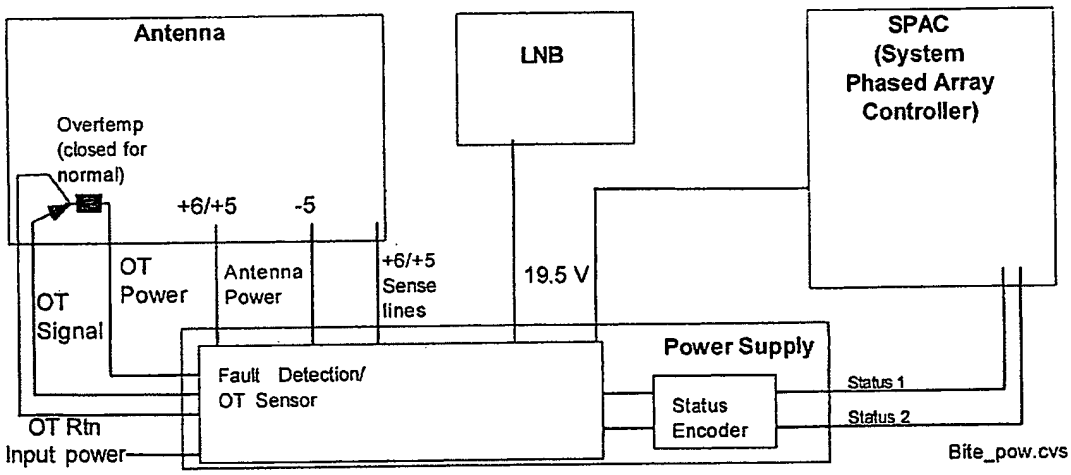


FIGURE 3.4-1. BITE CONCEPT FOR POWER

Over-temperature Monitoring. The power supply continuously monitors the antenna for over-temperature. The antenna provides this status by a temperature-sensitive transistor that functions as a normally closed switch. The switch opens when the temperature exceeds the local design point (based on maximum chip-back temperatures and the associated temperature at the monitor), and the "OT Signal" rises to +5V DC. When the power supply receives an indication of over-temperature it shuts down all antenna power and simultaneously provides a continuous status to the SPAC that power to the antenna has been disabled due to over-temperature. The SPAC displays this "over-temperature" operational status. When antenna normal operating temperature returns, the power supply provides power to the antenna (no need to reset power supply input power).

Power Monitoring. In the absence of the antenna over-temperature signal, the power supply provides the required voltage and current to the antenna, and monitors the outputs for under-current (which indicates an open cable or loss of one or more antenna panels), over-current (which indicates a short in either a cable or one or more antenna panels), and over-voltage or under-voltage (which, in the absence of an external short-circuit, are due to power supply faults, including self-induced shut down due to power supply internal over-temperature, or due to shorting or opening of voltage sense lines from the antenna). The power supply indicates an antenna power fault to the SPAC, which then associates loss of RF with the status provided by the power supply. The SPAC displays and reports an indication of "antenna power fault".

Because of the very low minimum current of the –5V line to the antenna (45 mA during loss of SPAC-antenna communications), undercurrent monitoring is absent on this interface. Loss of –5V to the antenna causes loss of communication between the SPAC and the EBSCs in the antenna, and is reported as a loss of beam steering control.

Current and voltage faults of the 19.5V DC (SPAC/LNB) power cause a shut down of all system power (antenna, LNB, SPAC). Faults of the power supply status to the SPAC are ignored unless there is an associated loss of RF as detected by the SPAC.

All power system faults (except antenna overtemperature) are latched by the power supply. This requires that the 115V AC power supply input power be reset (off-on) to clear the fault and allow the power supply to attempt to operate normally again.

3.4.2 Electronics

Figure 3.4-2 indicates the operational and fault monitoring features of the PACAS electronics.

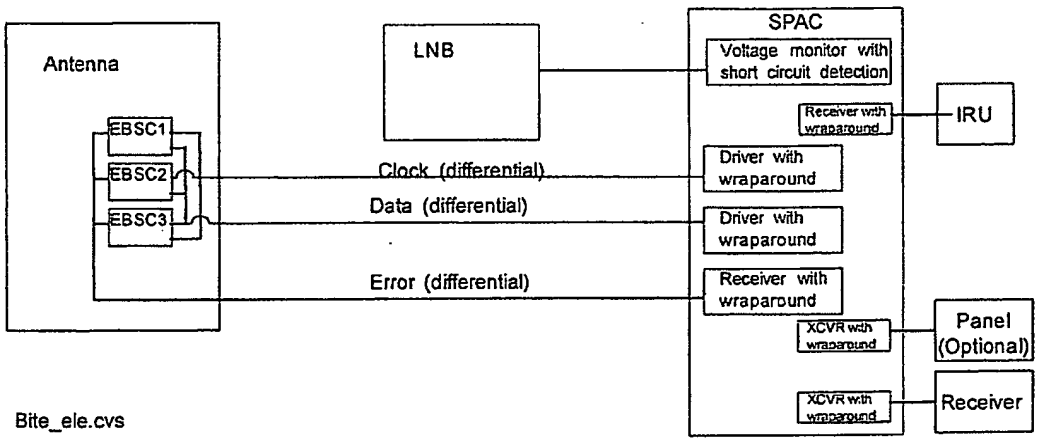


FIGURE 3.4-2. BITE CONCEPT FOR ELECTRONICS

The SPAC is intimately tied to the antenna steering/phasing electronics through a set of data lines. The antenna electronics have parity detection, which can be used to detect single-bit errors. The architecture of the electronics in the antenna precludes fault isolation to the antenna except when configuration or phase compensation data stored within the antenna is corrupted. All other

SPAC-antenna interface problems that fail to be isolated to the SPAC (using wrap-around tests) have indeterminate isolation (failure could be within antenna, SPAC, or interconnecting cable).

All SPAC external interfaces have self-test or wrap-around features. Upon detecting a loss of operational function (*i.e.*, fails to receive), the SPAC performs intrusive tests on the associated interface to determine whether the fault is inside the SPAC.

3.4.3 RF Monitoring

The BITE concept for RF uses the operational RF power monitors in the SPAC to detect low absolute power levels entering the SPAC (figure 3.4-3). Loss of RF at the SPAC may be due to loss of input from the satellite, antenna, LNB, SPAC, or cable failures (the ambiguity group for loss of RF).

Upon detecting loss of RF, the SPAC initiates intrusive tests to isolate the failure using the operational and BITE monitors outlined in the above sections.

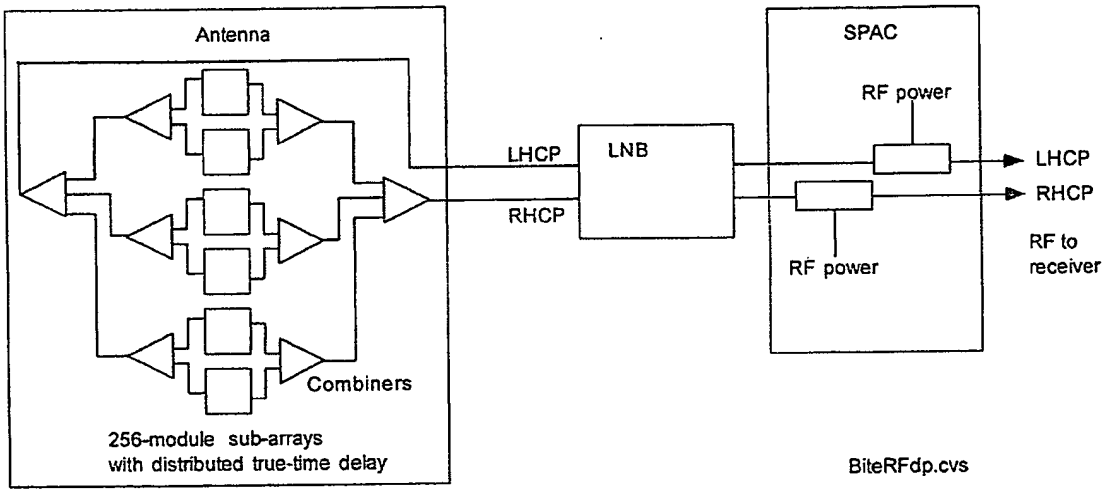


FIGURE 3.4-3. BITE CONCEPT FOR RF

4. LRU DESCRIPTIONS

4.1 Receive Antenna

This section describes the configuration of the Dual Polarization Receive (DPR) Antenna, pictured in figure 4.1-1. The functional block diagram is indicated in figure 4.1-2. A side-view of the various components of the antenna is displayed in figure 4.1-3.

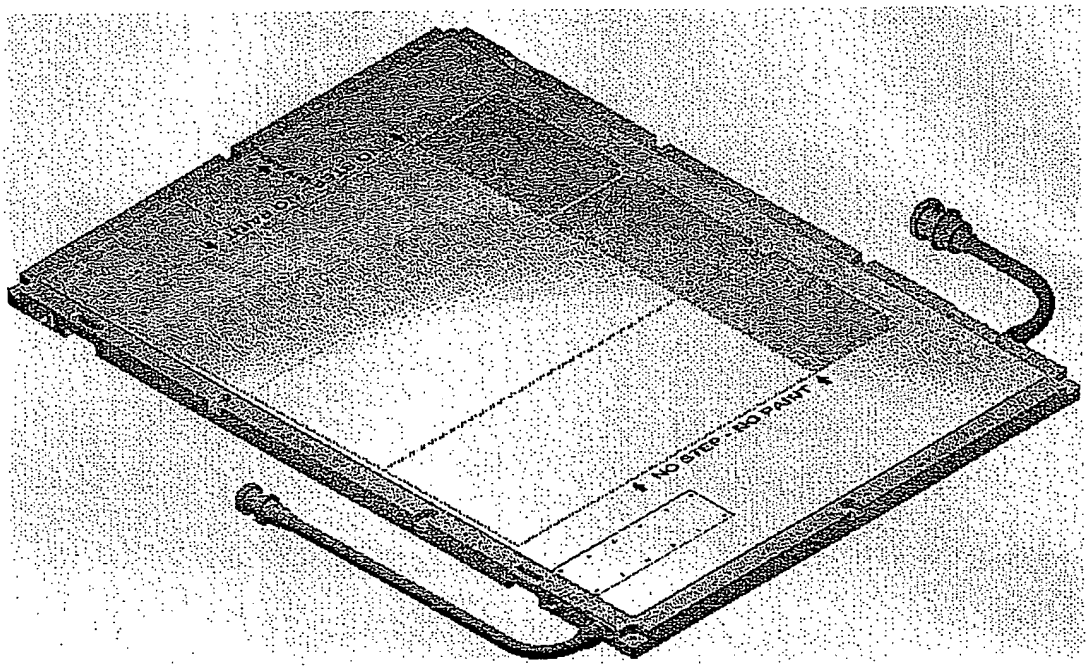


FIGURE 4.1-1. DUAL-POLARIZATION-RECEIVE ANTENNA

The overall size of the DPR antenna in approximately 37 inches long x 26.5 inches wide x 1.18 inches thick (reference figure 4.1-1). The weight is approximately 79 lbs.

It is broken up into 3 array subassemblies, each consisting of 505 electronic antenna modules, a Teflon based printed wiring board (TPWB) that combines the RF energy of these modules together and provides power and control circuitry, a machined aluminum enclosure with 505 counter-bored holes into which the modules fit, an aluminum pressure plate which holds the TPWB against the enclosure, an External Beam Steering Controller (EBSC) printed wiring assembly, and 4 True Time Delay (TTD) electronic modules that are used to amplify and correctly phase the RF outputs. These 3 Array subassemblies are bolted into a machined waveguide brazement. A wire harness, bus bar, and top and bottom covers are added to complete the assembly. Although the antenna is physically divided into 505 element blocks, functionally it is divided into 256 element blocks called subarrays. Due to physical and mechanical requirements, a few modules are required to be left out of each subarray. There are 2 subarrays in each 505 element Array Subassembly.

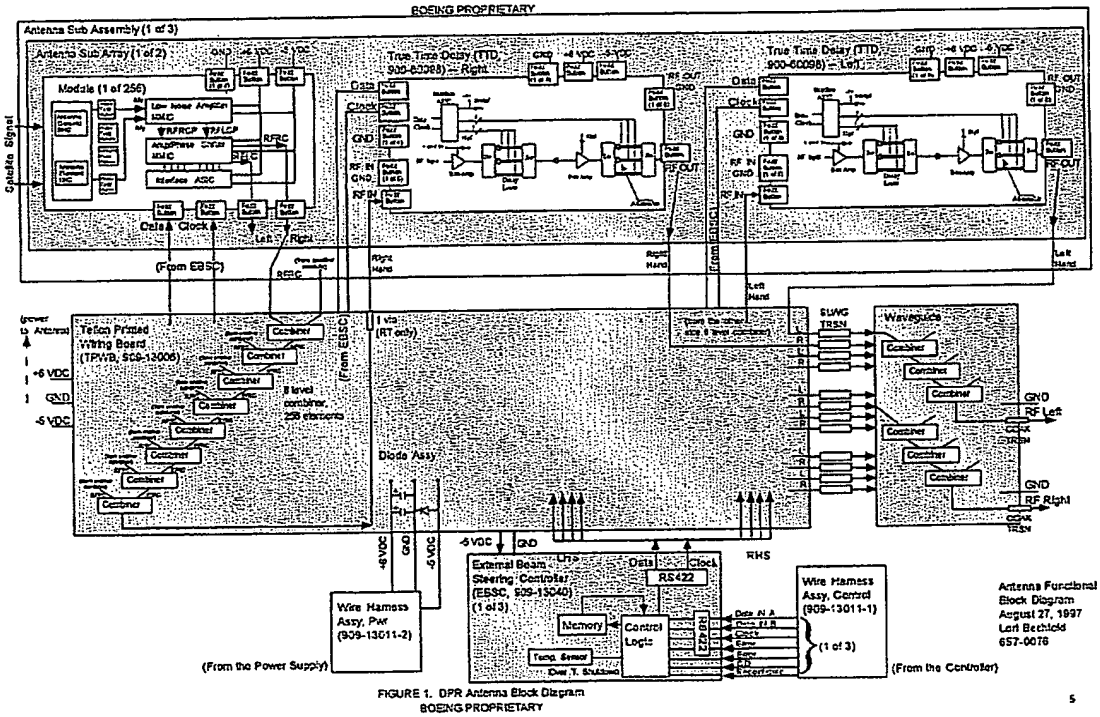


FIGURE 4.1-2. ANTENNA FUNCTIONAL BLOCK DIAGRAM

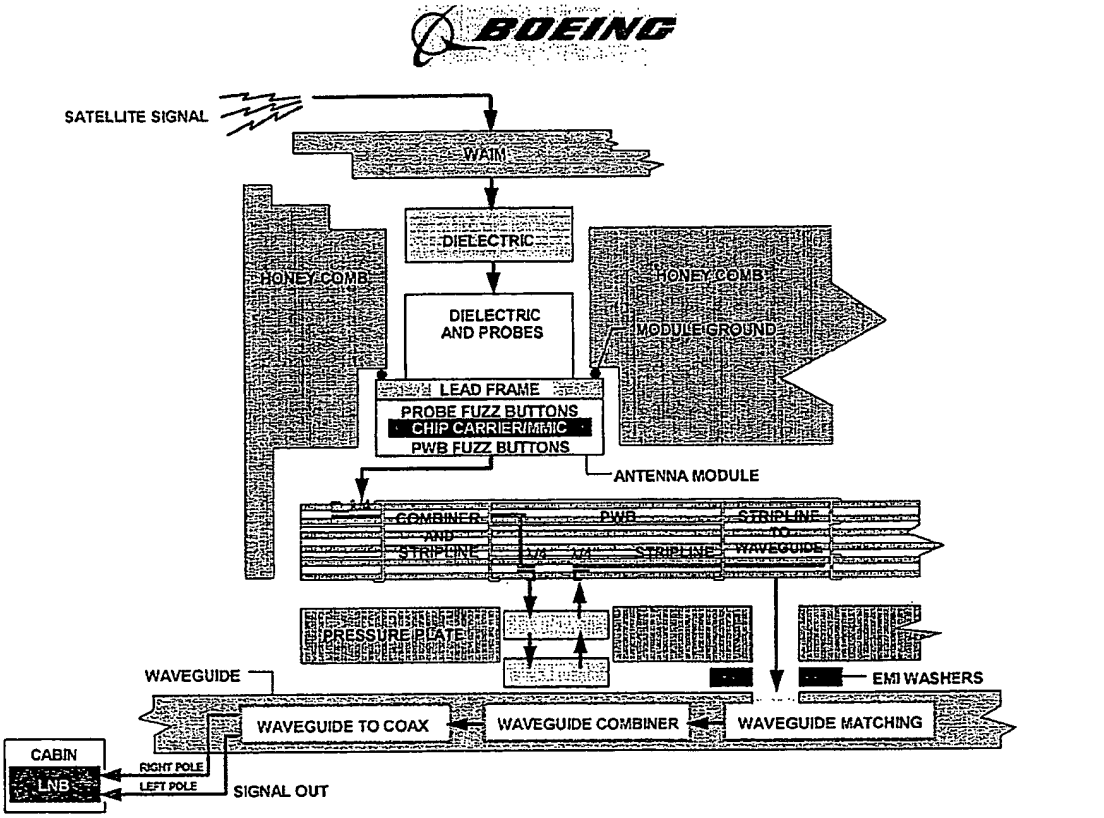


FIGURE 4.1-3. ANTENNA COMPONENTS (SIDE VIEW)

4.1.1 Antenna Modules

The module block diagram is indicated in figure 4.1-4. The module has the following characteristics:

- Two polarizations available simultaneously, LHCP & RHCP
- Independent steering control for each beam
- Chip set performance @ 12.7 GHz, (phase state 0, with bond wires)
- Gain ≅ 24.5 dB + 1.3/-2.3 dB
- Noise figure ≅ 1.34 dB +0.21/-0.11 dB
- Module performance is degraded TBD by packaging induced losses

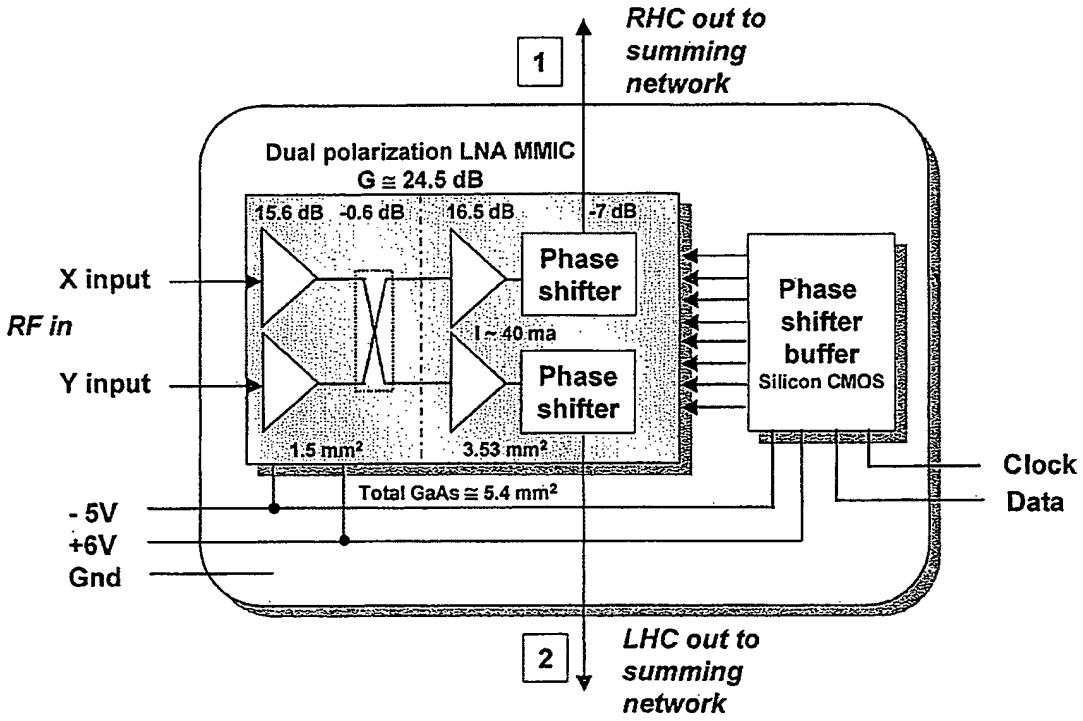


FIGURE 4.1-4. ANTENNA MODULE BLOCK DIAGRAM

Each antenna module (reference figure 4.1-5) is a static sensitive, multi-chip module, procured from Motorola, that is cylindrical in shape, approximately ½" diameter and 1/3" tall. The interconnection of the module to the TPWB is made with 10 fuzz buttons located on one end of the cylinder. These are solder-less pressure connections that are very small and fragile. Each fuzz button is a 0.020"-diameter cylinder that is 0.052" tall made of a long, 0.001"-diameter gold wire which is crinkled up into the cylindrical form factor.

Internal to the molded probe are two antenna elements which pick up the RF energy from the satellite. This energy is then transferred into the ceramic chip carrier where it is amplified and controlled and then transferred into the TPWB.

The ceramic chip carrier contains Boeing designed amplifiers, phase shifters, and an interface ASIC as shown in figures 4.1-6 and 4.1-7.

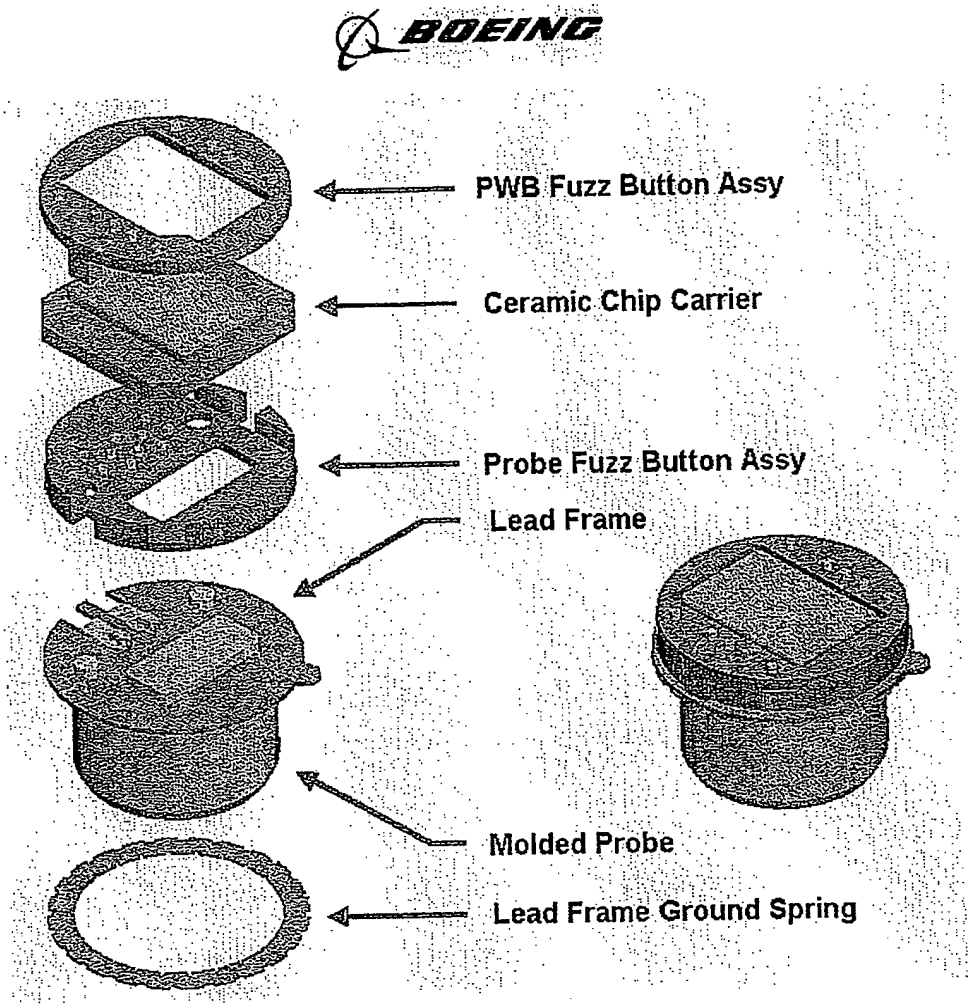


FIGURE 4.1-5. ANTENNA MODULE ASSEMBLY

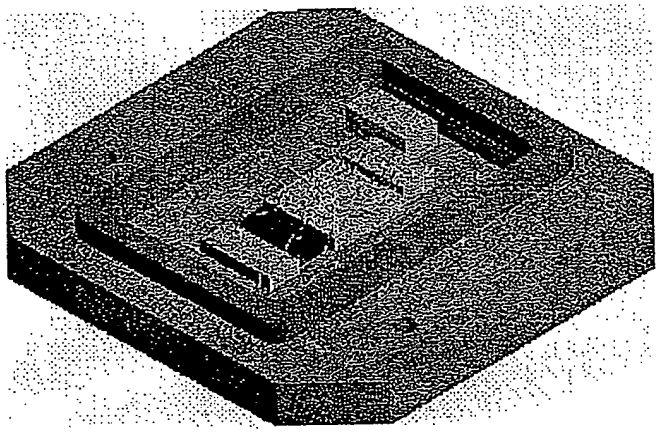


FIGURE 4.1-6. ANTENNA MODULE CHIP CARRIER

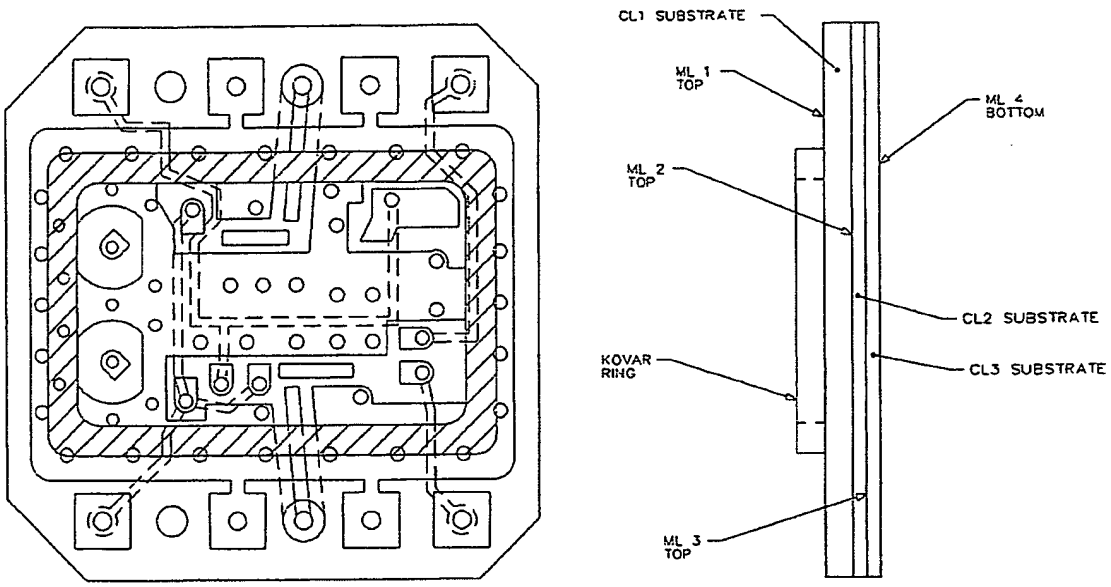


FIGURE 4.1-7. ANTENNA MODULE CHIP LAYOUT

4.1.2 Module Enclosure Assembly

The module enclosure assembly consists of a machined aluminum detail (see figure 4.1-8) approximately 21" long x 7.75" wide x 0.591" thick with 505 precision reamed holes in it. Each hole is partially filled with a dielectric plug which is mounted flush with the top of the enclosure. A composite panel (Wide-Angle Impedance Matching aperture or "WAIM") is then bonded to the top of the enclosure and the top of each plug (see figure 4.1-6). For protection during transportation, a protective thick and tough pressure sensitive paper is applied to the top of the WAIM. This protective paper is removed prior to test. The assembly is required to be handled in such a fashion as to prevent scratches to the WAIM.

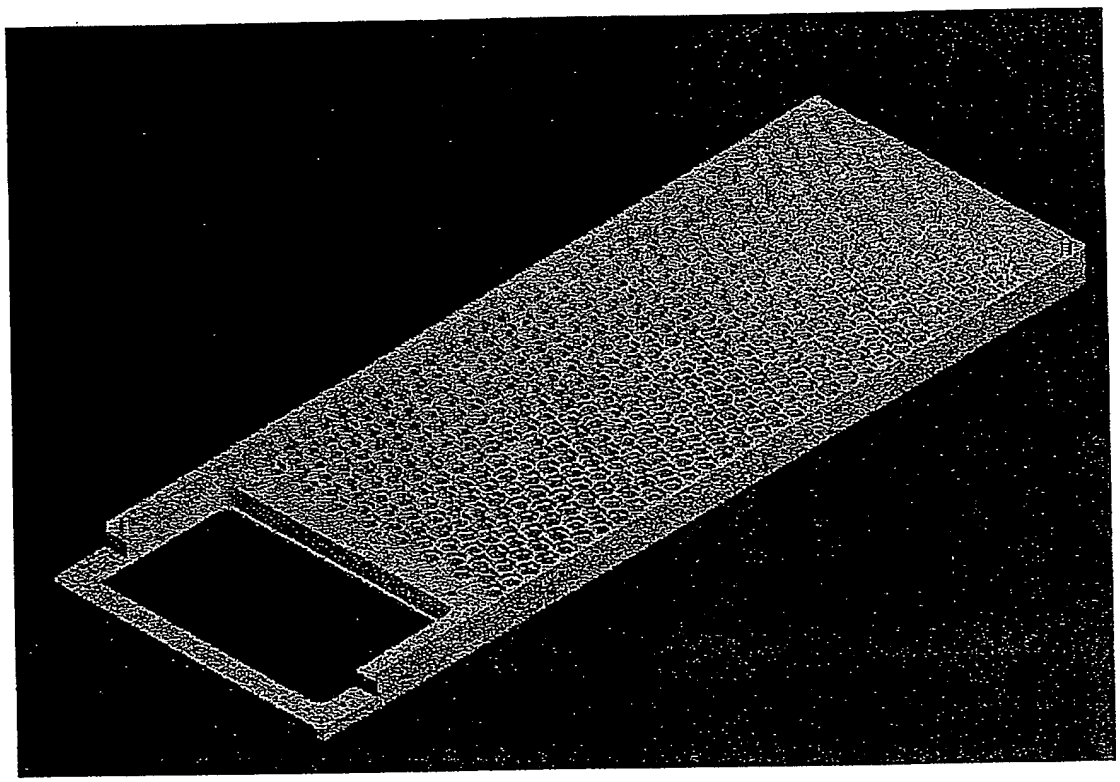


FIGURE 4.1-8. ANTENNA MODULE ENCLOSURE

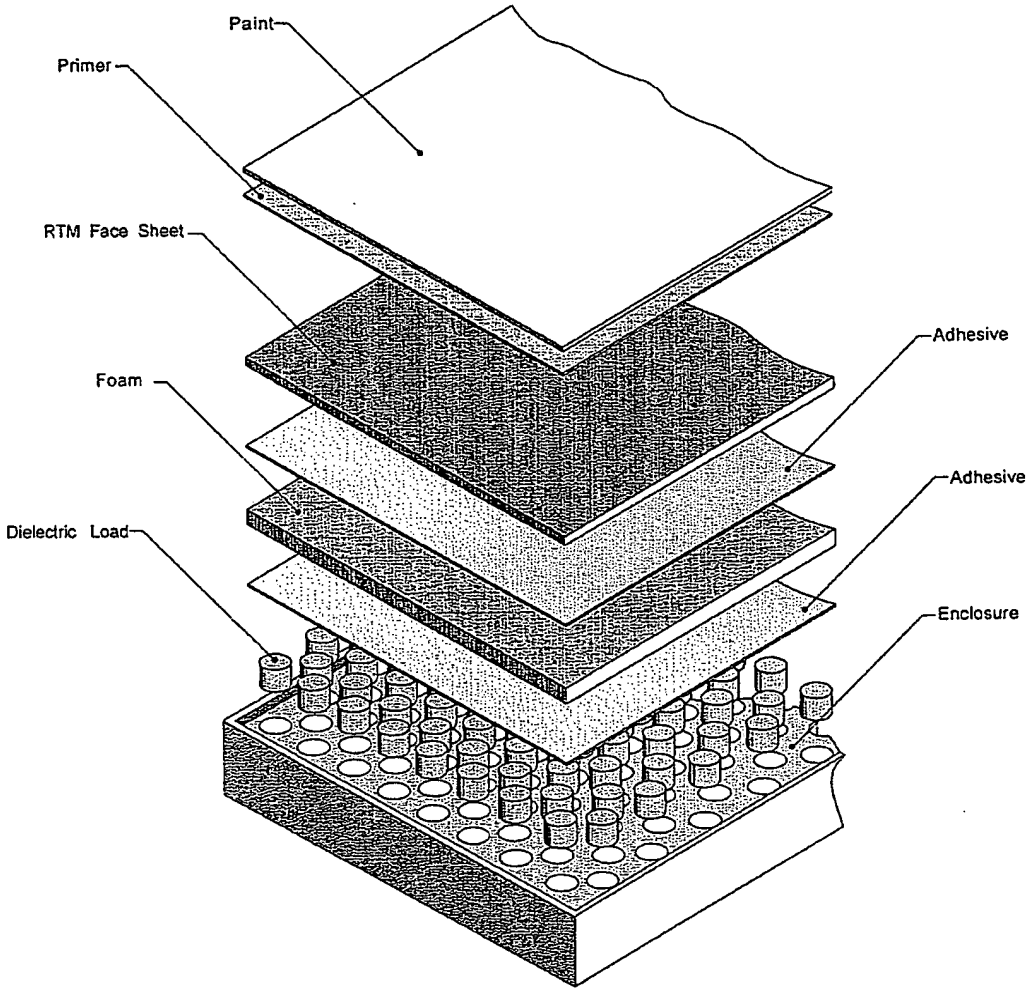


FIGURE 4.1-6. WAIM LAYERS

4.1.4 Teflon Printed Wiring Board Description

The TPWB is approximately 21" long x 7.75" wide x 0.115" thick. It is primarily gold plated on all surfaces with surface mount pads on layer 1 that interface with the Antenna Module fuzz buttons. It is a 12-layer board with internal screened-on resistors as well as internal RF layer-to-layer couplers and combiners. There are 3/16 tooling pin holes in opposite corners for aligning the TPWB to the Module Enclosure Assembly, one of which is a tight, locational-clearance fit for precisely locating the board, with the second slightly looser to allow for tolerances. Energy from the antenna modules comes into the TPWB where it is combined and "launched" into the waveguide through internal probes.

4.1.5 Waveguide

The waveguide is a machined aluminum brazement that acts as the main chassis structural component of the antenna as well as the RF waveguide. It is approximately 37" long x 26.5" wide with the thickness varying from 0.25" over the majority of the center portion to 1.18" thick

near the edges (see figure 4.1-7). There are 6 "ports" or launch points into the waveguide for each polarization, one for each subarray. These 6 RF inputs are combined internally to a single output. Each output, Left Hand Circular Polarization (LHCP) and Right Hand Circular Polarization (RHCP) is feed into a probe which transitions to an SMA coaxial connector.

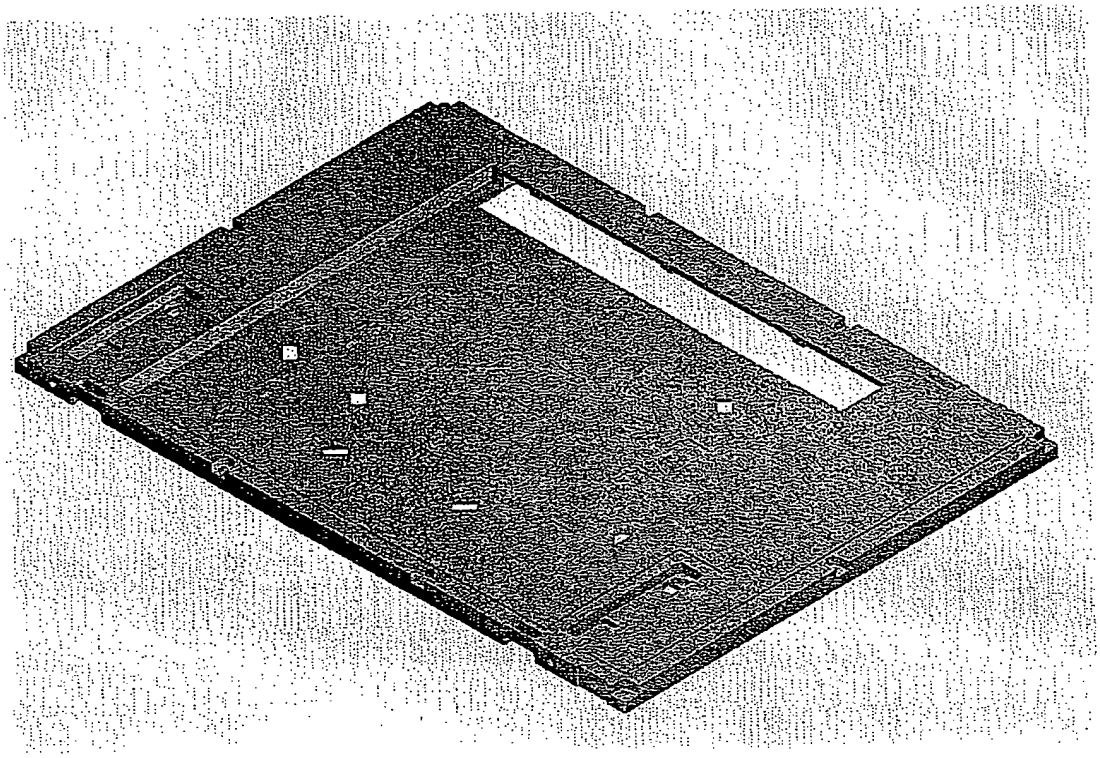


FIGURE 4.1-9. WAVEGUIDE

4.1.6 Wire Harness Descriptions

There are 2 wire harness assemblies, Controller and Power, and 2 semirigid coax cable assemblies, RHCP and LHCP, in the antenna. Each exits the antenna on the side (1.18" thickness). For the wire harness assemblies, since the antenna side is too thin to mount the necessary connector on it, the antenna has "flying" wire bundles exiting it. The Controller Wire Harness is built as a harness with only the contacts installed on the outside connector wire ends (no connector). The harness will be completed on assembly by inserting the wires through a side hole in the antenna and installing the connector.

The controller wire harness consists of 8 twisted shielded pairs (AWG 20) terminated inside the antenna to M55302/66 style crimp connectors (one at each EBSC). Daisy-chain type wiring connects the EBSC PWAs and is manufactured on a standard form board.

The Power wire harness consists of 2 (AWG 4) wires, 2 twisted shielded pairs (AWG 20), 1 twisted pair (AWG 12) and 1 twisted triad (AWG 20), terminated inside the antenna to terminal lugs.

4.1.7 Bus Bar Description

The bus bar (reference figure 4.1-10) consists of 3 machined copper strips, laminated together with insulators between the conductors for isolation. There are 6 studs at each TPWB location, 2 for each voltage (+V, -V, Gnd) and studs at one end for connecting the Power wire harness terminal lugs.

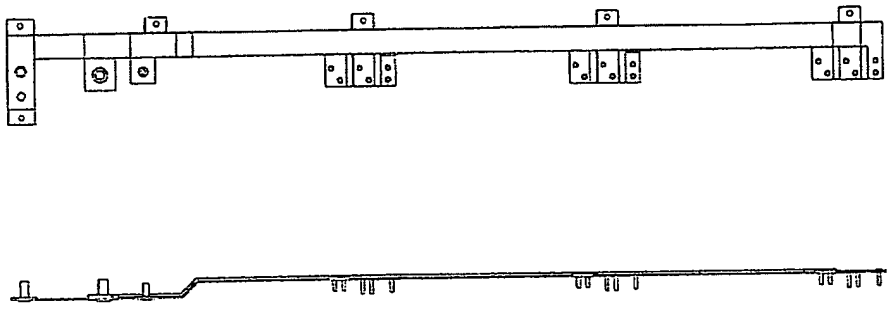


FIGURE 4.1-10. BUS BAR

4.1.8 TTD Module Description

The TTD or True Time Delay Module is a static sensitive, 1.25-inch square electronic module as shown in figure 4.1-11. It consists of a large custom substrate required for the necessary delay lines and a small chip cavity for the amplification and switching functions (figure 4.1-12). There is one TTD module for each polarization of each subarray. Since at high scan angles the RF signal strikes the near side of the antenna sooner than the far side, the TTD provides the proper delays such that all subarrays of one polarization are in phase with each other and the energy from each can be combined with the highest efficiency (reference section 3.3.3.3).

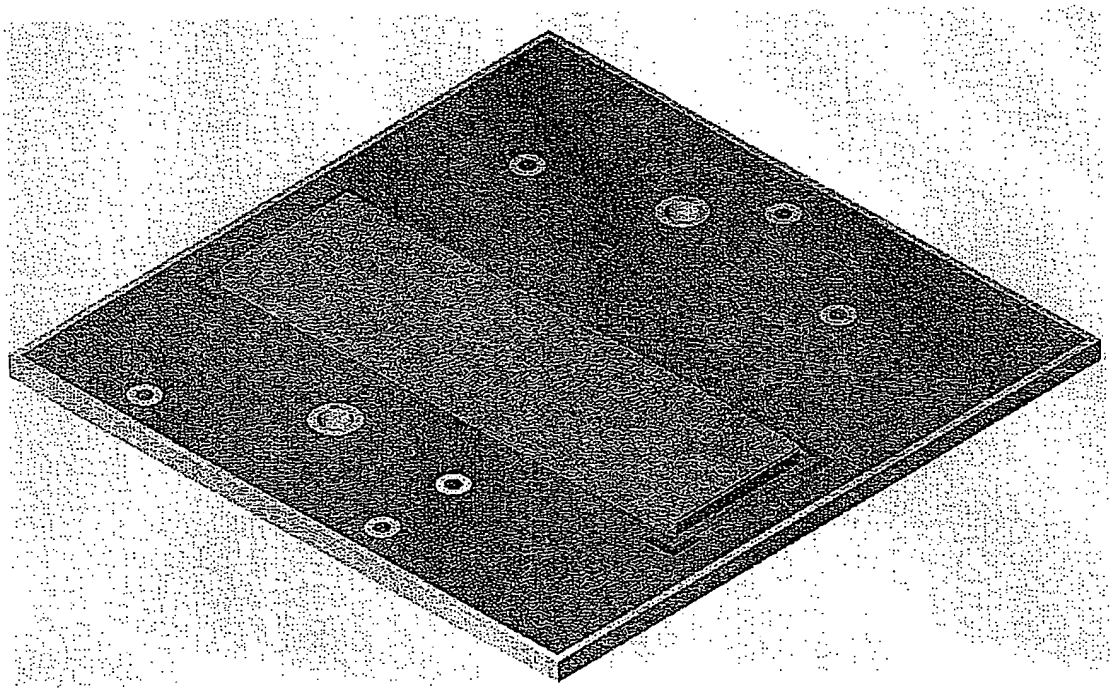


FIGURE 4.1-11. TTD MODULE

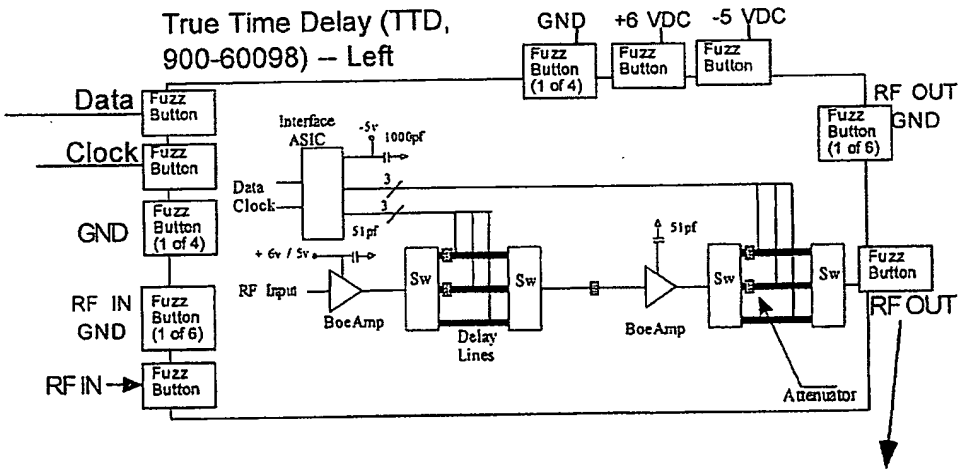


FIGURE 4.1-12. TTD MODULE SCHEMATIC

4.1.9 EBSC PWA Description

The EBSC (Electronic Beam Steering Controller) PWA provides the interface between the antenna and the SPAC as shown in figure 4.1-13. It is a 5" x 7" circuit card that interconnects to the TPWB via solder-less pressure-spring finger interconnects. The block diagram is indicated in figure 4.1-14.

The EBSC provides the control interface between the SPAC and the antenna modules and TTDs, receiving phase-shifter commands and TTD settings. It also retains antenna configuration data for downloading to the SPAC, and provides temperature status to the power supply for shutdown on overtemperature.

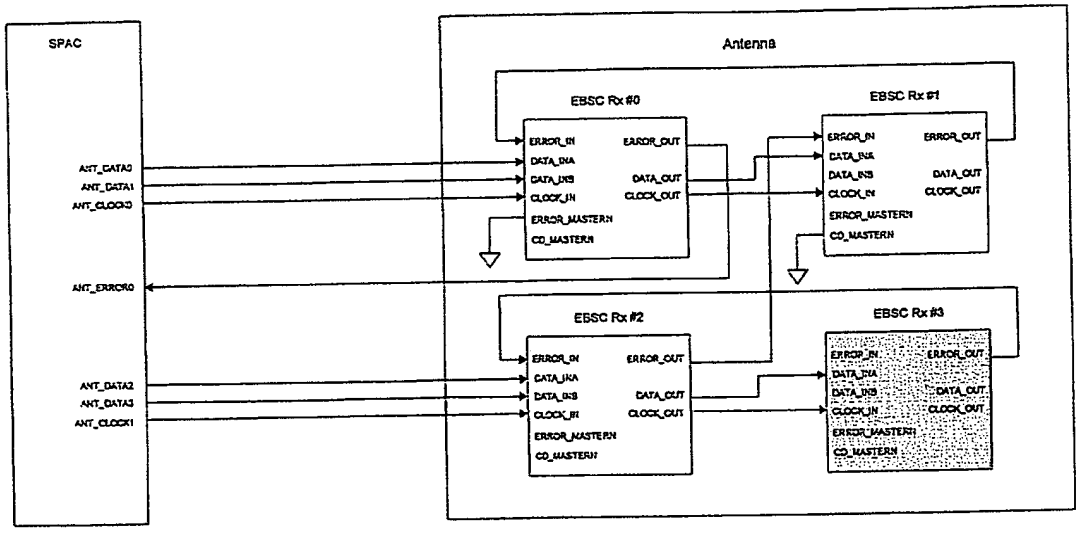


FIGURE 4.1-13. EBSC-SPAC INTERFACE

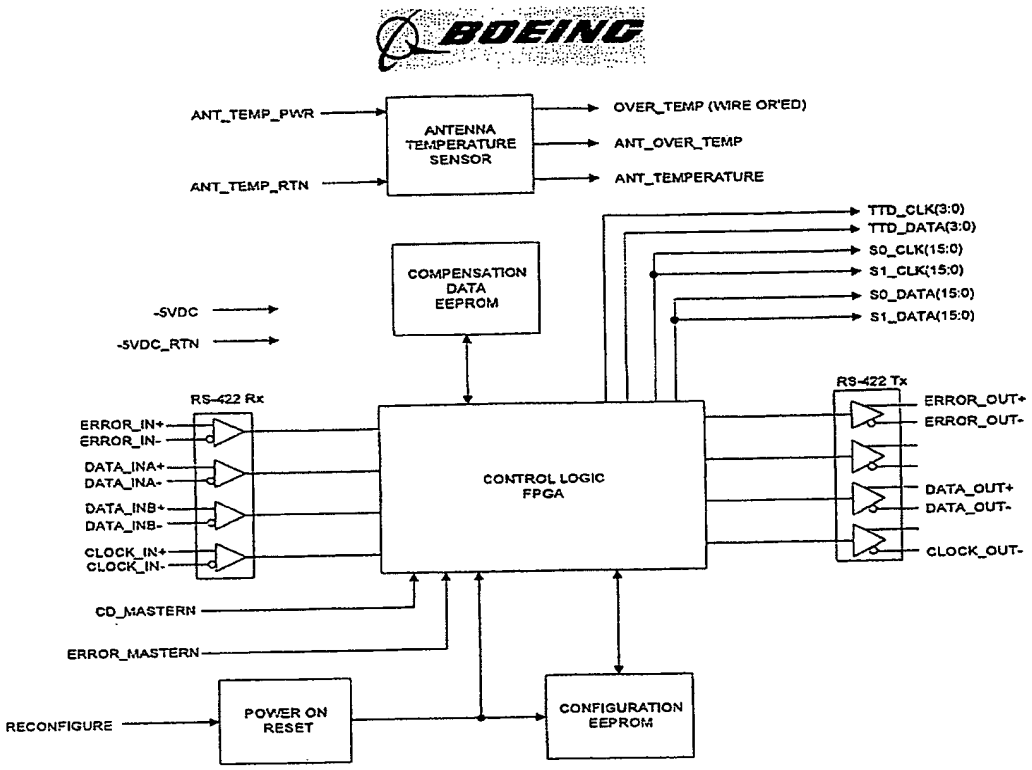


FIGURE 4.1-14. EBSC BLOCK DIAGRAM

4.2 Low-Noise Block/Down Converter

The PACAS low-noise block/down converter (LNB) receives dual polarity, RHCP and LHCP, Ku-dual-band frequency inputs from the antenna and converts them (independently) from either 11.7-12.2 GHz or from 12.2-12.7 GHz into an IF of 950-1450 MHz, the IF band suitable for FSS demodulators and DBS receivers (see figure 4.2-1). The converted Ku band is delivered to the SPAC at IF.

Band selection for the LNB (11.7-12.2 or 12.2-12.7 GHz band) is supplied from the SPAC using DC levels multiplexed onto the output IF coax via the coax center conductor. The specific DC level determines which of the two bands, DBS or FSS, are to be converted (selected). Two separate Ku receive channels are maintained: one for RHCP and one for LHCP, one or both for DBS and one or both for FSS. The functional requirements apply independently to each channel. Power is supplied from the power supply at 19.5V DC via a 3-pin circular power connector mounted on the LNB package.

The LNB is procured as a development item from Satellink, Inc., of Dallas, Texas. Dimensions are approximately 4" x 6" x 8", and the weight is approximately 6 lbs.

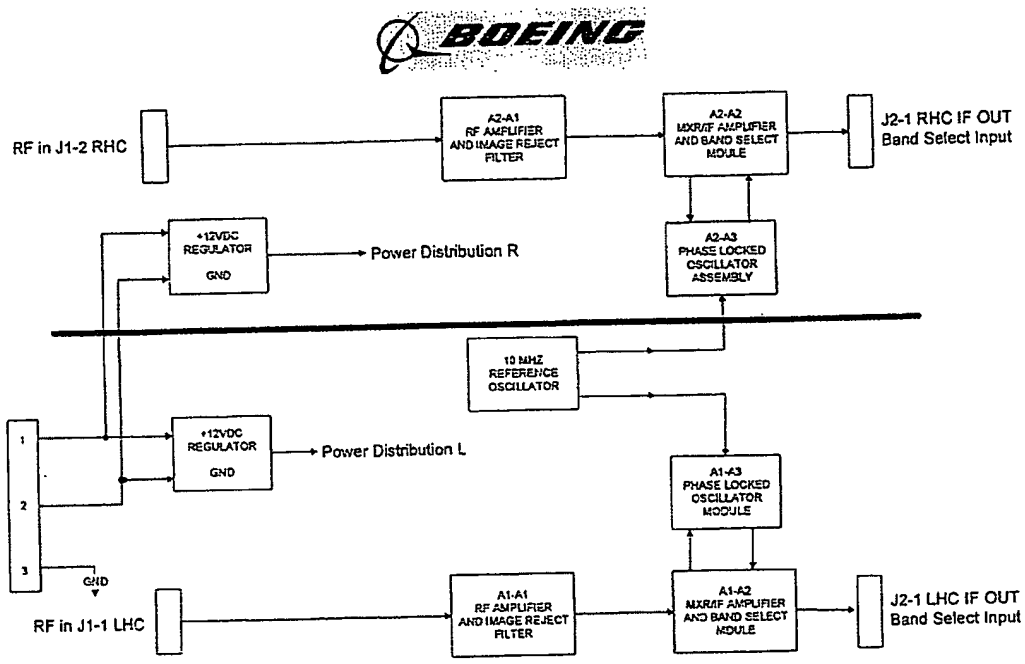


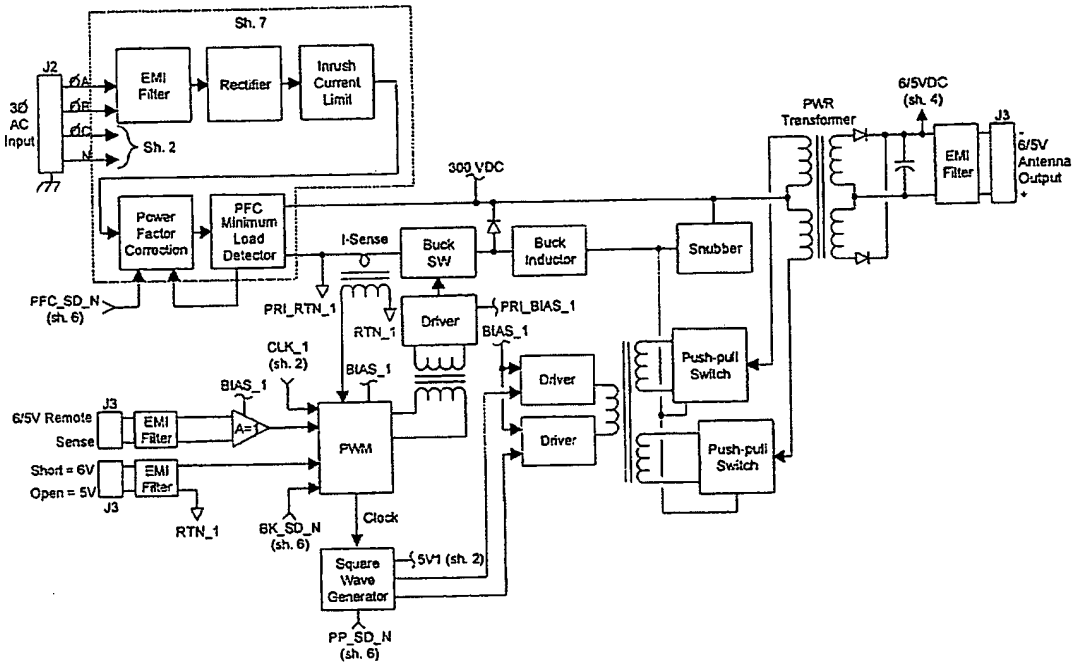
FIGURE 4.2-1. LNB BLOCK DIAGRAM

4.3 Power Supply

The Phased Array Power Supply provides electrical power to the other elements of the PACAS. It converts 115V, 3 Phase, 400 Hz airplane power to three DC voltages and an antenna overtemperature sensor supply needed by the system. The voltages and currents are:

- +6 or +5V DC at up to 83 A (reference figure 4.3-1)
- -5V DC at up to 1.6 A (reference figure 4.3-2)
- +19.5V DC at up to 3 A (reference figure 4.3-2)
- +7.5V DC at 4 mA (nominal) for antenna overtemperature (reference figure 4.3-3)

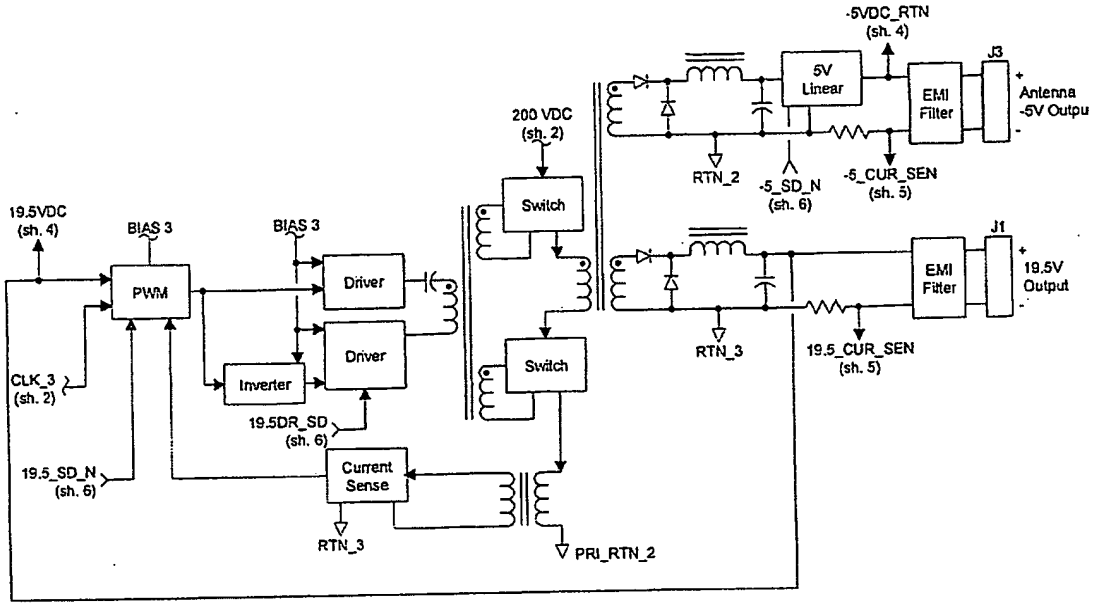
The +6/5V output has remote sense capability to overcome voltage drops due to the high current load (figure 4.3-1).



Input and 5/6V Antenna Converter
(schematic pages 2.0, 2.2, 2.3, 2.4, 2.5)

Sheet 1 of 7

FIGURE 4.3-1. PS BLOCK DIAGRAM: INPUT AND 5/6V ANTENNA CONVERTER



19.5V & -5V Converters
(schematic pages 2.10, 2.11)

Sheet 3

FIGURE 4.3-2. PS BLOCK DIAGRAM: 19.5V& -5V CONVERTERS

From the auxiliary supply (figure 4.3-3) the power supply provides power to, and monitors the output of three temperature sensors inside the antenna (figure 4.3-4).

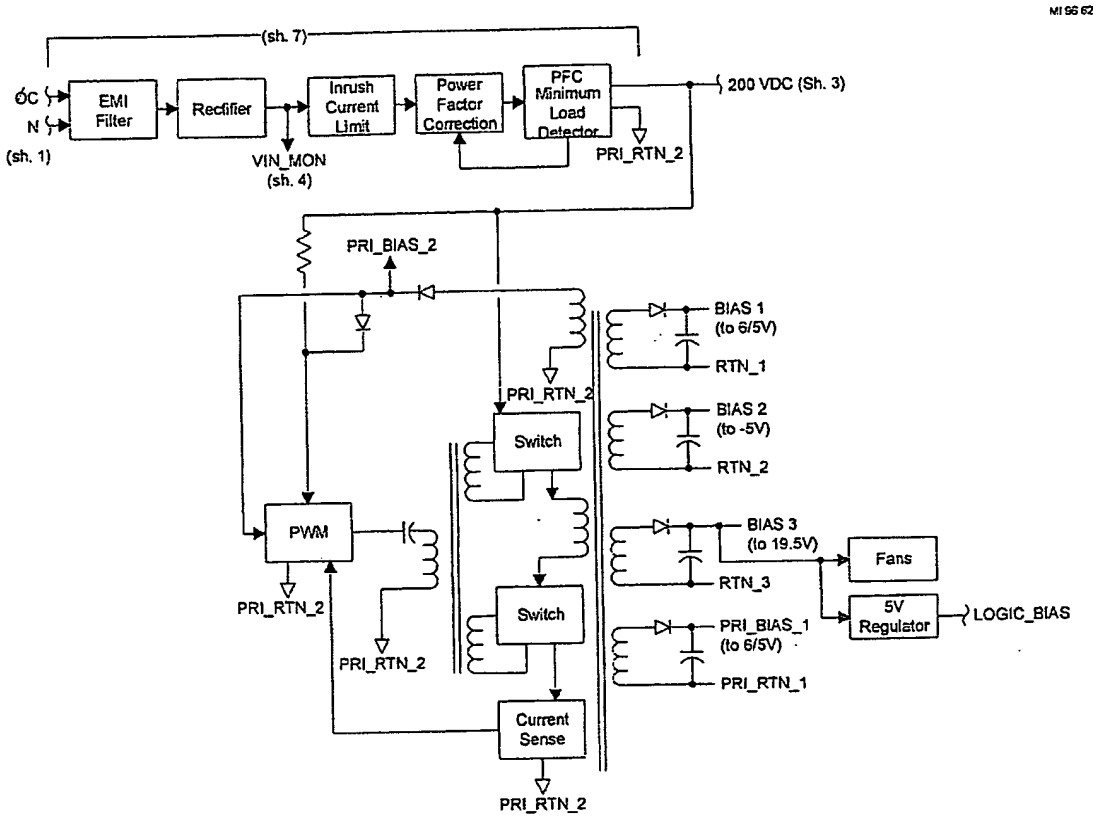
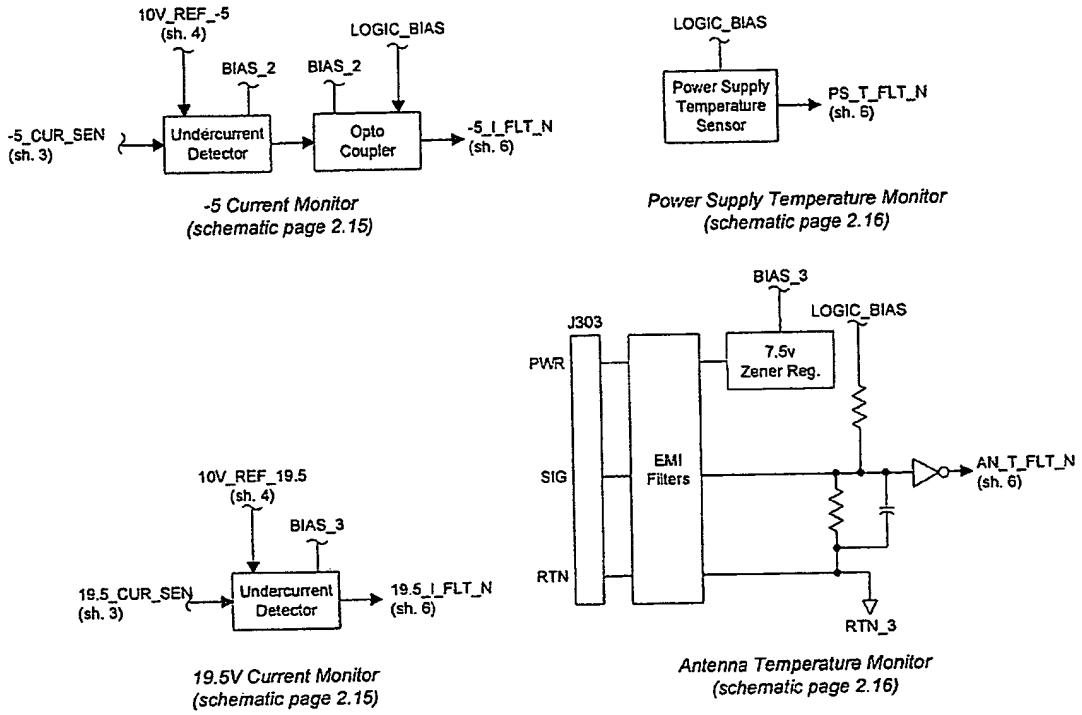


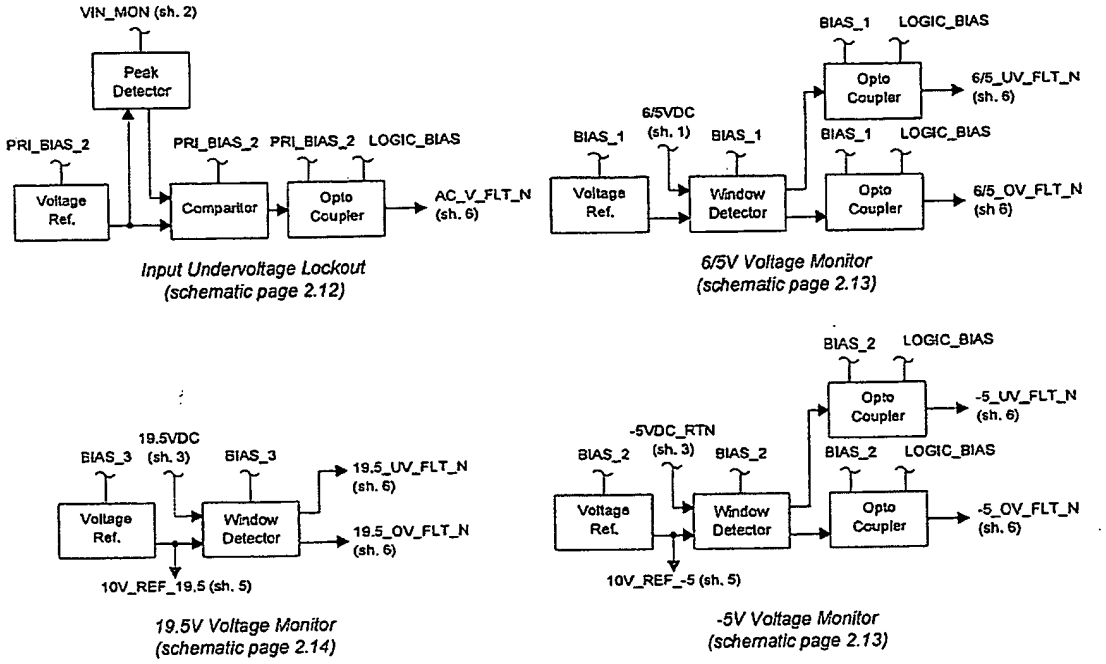
FIGURE 4.3-3. PS BLOCK DIAGRAM: AUXILIARY SUPPLY



Current and Temperature Monitors Sheet 5

FIGURE 4.3-4. PS BLOCK DIAGRAM: CURRENT AND TEMPERATURE MONITORS

The power supply also monitors for over/under voltage, and out-of-range current conditions on all outputs (figures 4.3-4 and 4.3-5).



Sheet 4

FIGURE 4.3-5. PS BLOCK DIAGRAM: VOLTAGE MONITORS

Power supply status is synthesized in the logic circuits (figure 4.3-6) and transmitted to the SPAC as a two-bit status word. The four status conditions are:

- No Faults
- Antenna Power Fault
- Controller/LNB Power Fault
- Antenna Overtemperature

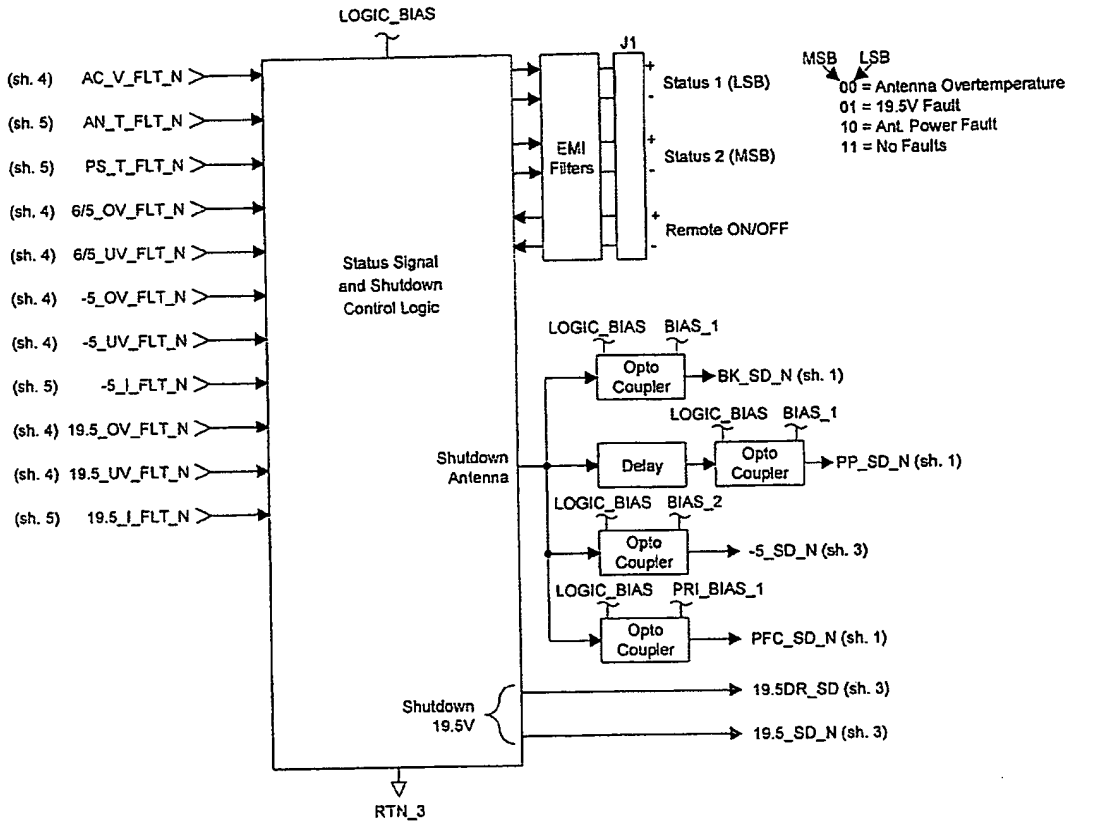


FIGURE 4.3-6. PS BLOCK DIAGRAM: MONITOR LOGIC

The power supply shuts down power to the antenna in the event of an antenna overtemperature or a fault in the +6/5V or -5V power, but leaves SPAC power intact. The power supply shuts down all output power in the event of a fault in input power or the 19.5V output, which powers the SPAC/LNB. Among these faults, antenna overtemperature causes power to cycle to the antenna; the other faults are latched until power supply input power is cycled.

The power supply external dimensions are 18 x 10 x 3.5 inches (figure 4.3-7). It weighs approximately 18 lbs. and has a carrying handle for convenience. Two fans cool it.

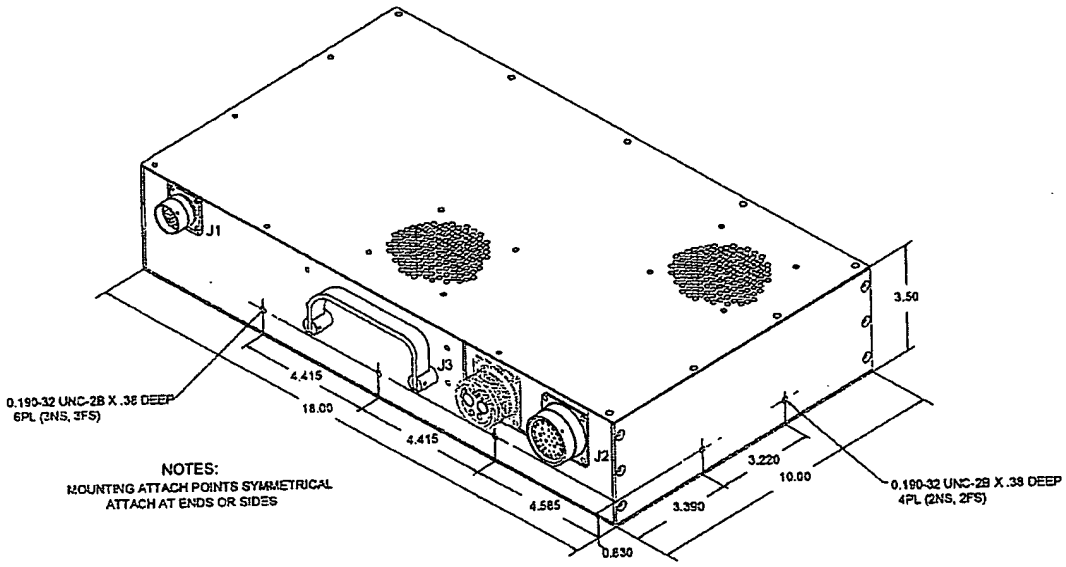


FIGURE 4.3-7. POWER SUPPLY

Internally, the power supply consists of three major assemblies, the printed wiring assembly (PWA), the input filter module, and the output filter module. The PWA contains three test connectors, one of which is accessible through the enclosure for signals used during the functional test procedure. The power factor correction circuitry is shown in Figure 4.3-8.

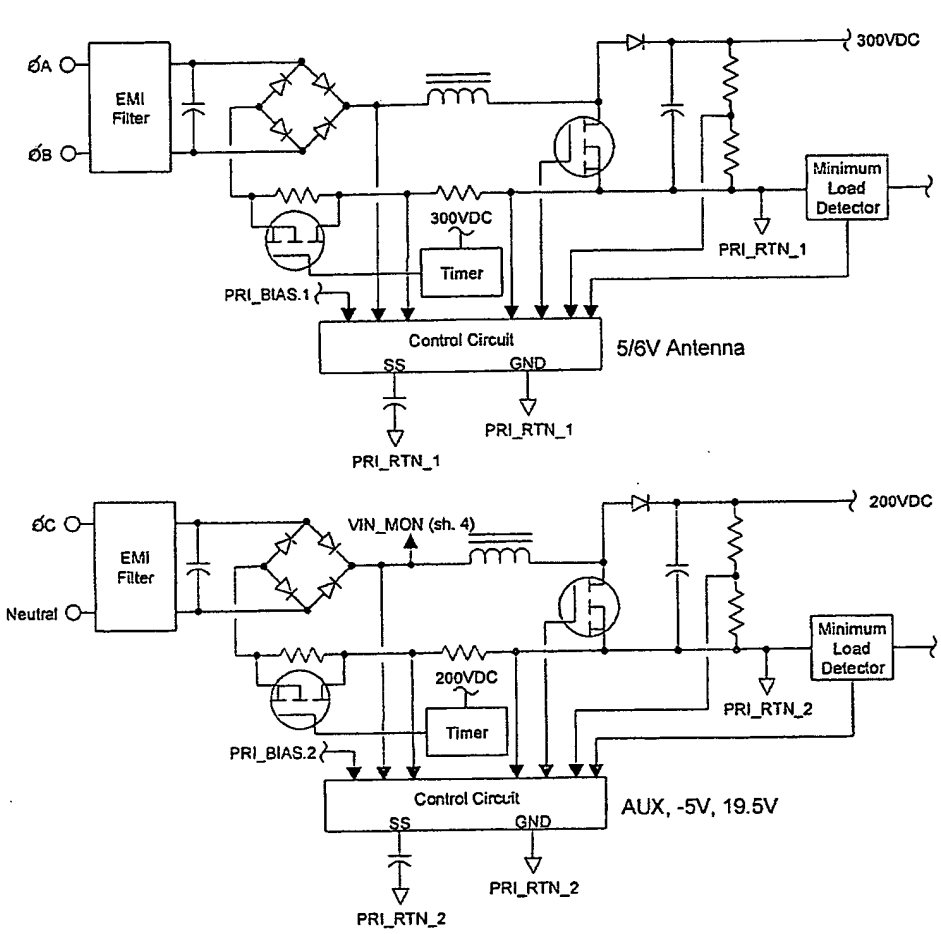


FIGURE 4.3-8. PS BLOCK DIAGRAM: POWER FACTOR CORRECTION

4.4 System Phased Array Controller

The PACAS system phased-array controller (SPAC) provides control and external status of PACAS functions (reference STARS-CKTS-CONT-002). The SPAC interfaces with the external receiver, ARINC 429 inertial reference, and optional external status interface. The SPAC controls the antenna module pointing for each of two beams by calculating and transmitting the relative phases of each module to the antenna, and controls the true-time delay units in the antenna via the same beam-pointing digital interface. The SPAC also performs status and fault consolidation for fault isolation.

Figure 4.4-1 shows a possible connection diagram using the system phased array controller (SPAC) (reference figure 4.1-13 for the antenna digital interface). In this example the SPAC is controlling both a transmit and a receive antenna. The hardware has the necessary interfaces to control two antennas, however software to control only the receive array has been written.

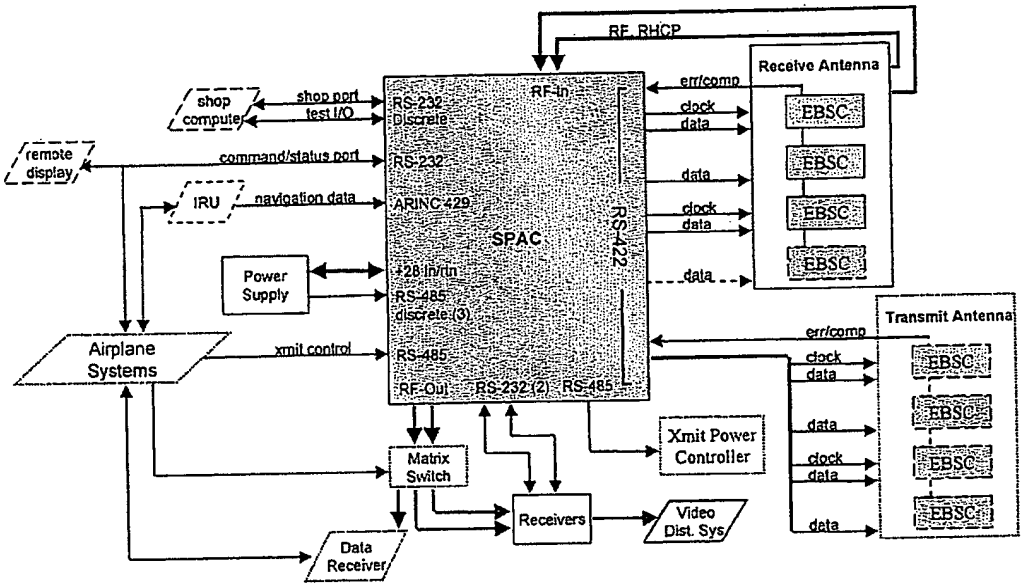


FIGURE 4.4-1. SYSTEM PHASED ARRAY CONTROLLER CONNECTION EXAMPLE

4.4.1 SPAC Architecture

The SPAC consists of two PWAs, one digital and one RF, mounted in a custom chassis tailored for optimum heat dissipation. The two cards are connected via a ribbon cable with filter pins mounted to an RF shield plate. Mating connectors are mounted on the cards; there is no backplane in the design. The external dimensions are 4" x 15" x 11", and the weight is approximately 7.5 lbs. Figure 4.4-2 shows the SPAC components (SK version).

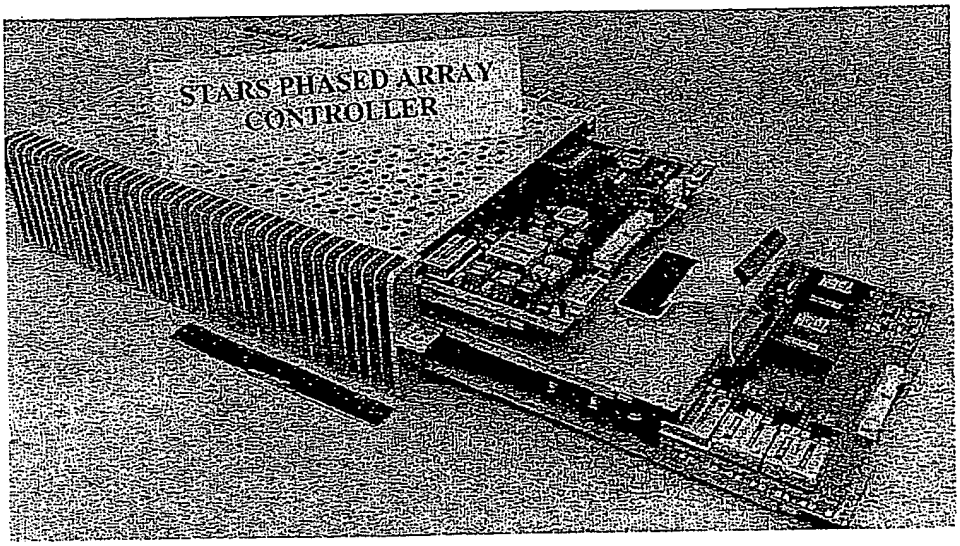


FIGURE 4.4-2. SYSTEM PHASED ARRAY CONTROLLER

4.4.2 SPAC Block Diagram

A block diagram of the SPAC is shown in figure 4.4-3. The left side of the diagram represents the Processor/Data Calculator card while the right side depicts the RF detector PWA.

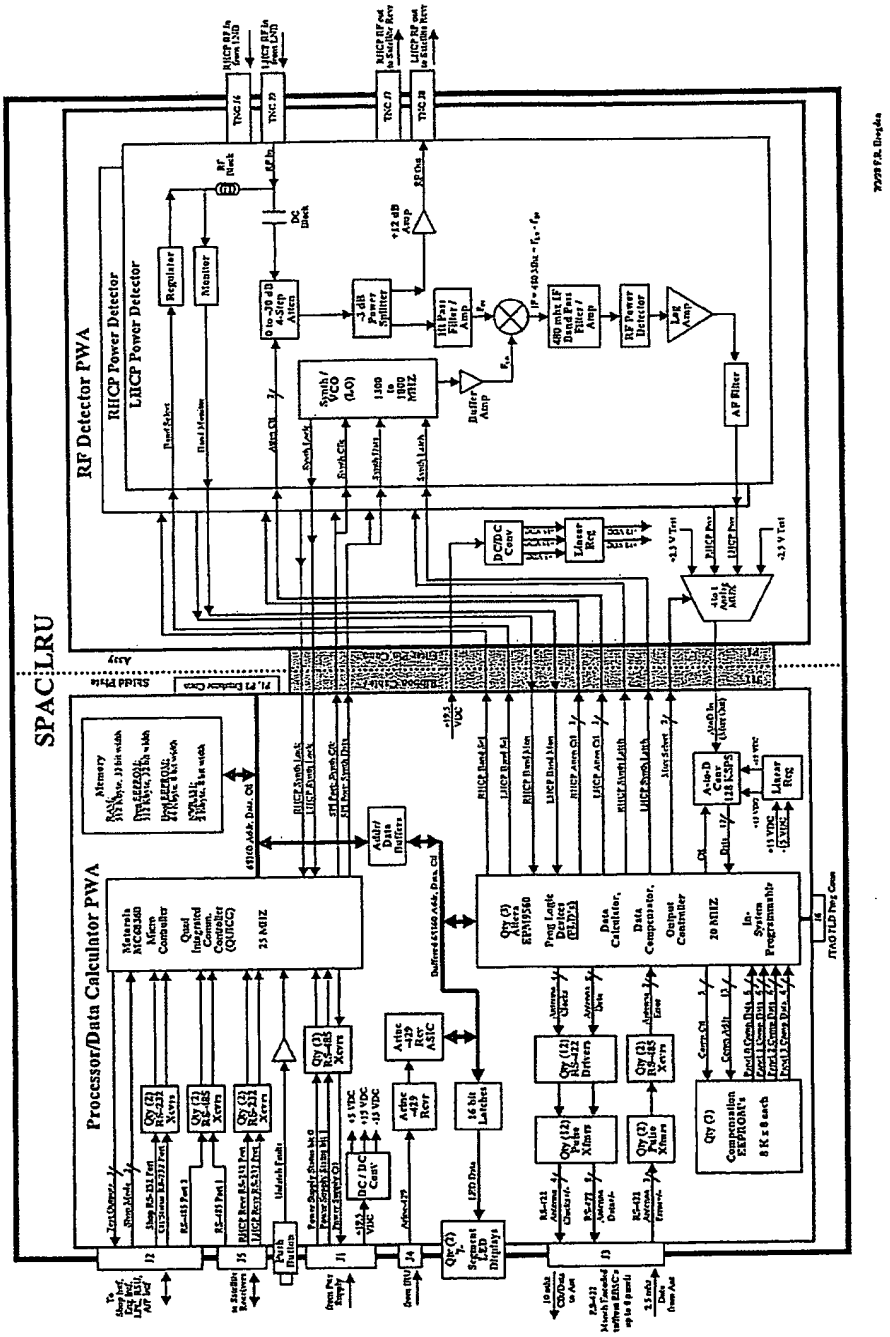


FIGURE 4.4-3. SPAC BLOCK DIAGRAM

The controller connects to the system via nine connectors as shown in table 4.4-1.

TABLE 4.4-1. SPAC CONNECTORS

Connector #	Function
J1	Power supply interface
J2	General purpose I/O – Shop RS-232 – Control/Status RS-232 – RS-485 port – 5 discrete I/O
J3	Antenna I/O – RS-422 out (12) – RS-422 in (2)
J4	ARINC-429 input
J5	Receiver I/O – RS-232 (2)
J6, J9	RF input (TNC)
J7, J8	RF output (TNC)

The connectors are soldered to the individual PWAs and exit through cutouts in the chassis.

Key features of the SPAC PWAs are described in the following paragraphs.

4.4.3 Digital Card Description

The digital card contains the processor, data calculator, program EEPROM, program RAM, and all of the digital interfaces for the SPAC. The card is pictured in figure 4.4-4.

The baseline parts list includes:

- 1 x MC68360, Quad integrated communications controller (QUICC).
- 128K x 32 bit, EEPROM for 68360 program store.
- 128K x 32 bit, RAM for the 68360.
- X20C16, Xicor 2K x 8 autostore NOVRAM, for non-volatile parameter storage.
- 3 x EPM9560, Altera MAX9000 family programmable logic devices implementing the data calculator, data compensator, and data formatter functions.
- 1 x Boeing ARINC-429 receiver ASIC
- Miscellaneous buffers, glue logic, and line drivers as required.

The RS-232 interfaces are three wires, TXD, RXD, and GND. The receiver RS-232 interfaces support the Thomson DSS-1 (for DirecTV and USSB) and EchoStar 6996 (for DISH Network) protocols.

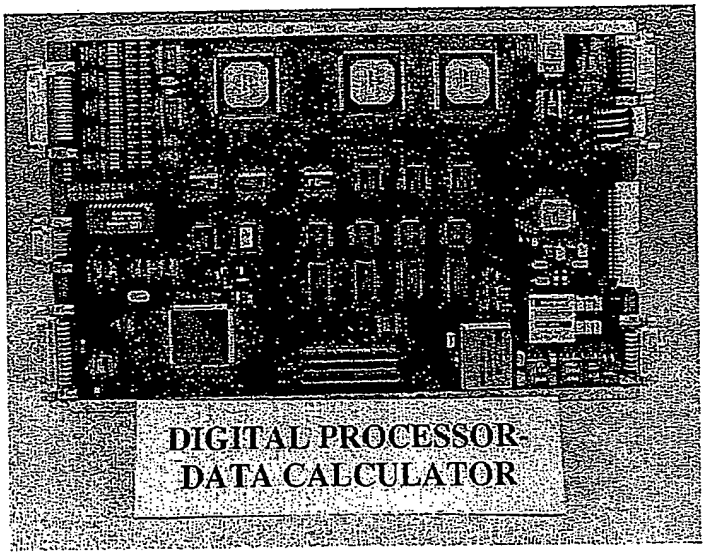


FIGURE 4.4-4. SPAC DIGITAL CARD SRU

4.4.3.1 Phase Calculation Circuits (reference D909-80054)

A primary function of the processor/data calculator card (PDC) is the computation of phase shifter settings for each element in the antenna. The PDC contains three high-density, erasable programmable logic devices (EPLD, Altera EPM9560s) that implement the data calculation, data compensation, and output formatting functions. A block diagram of the data calculation circuits is shown in figure 4.4-5.

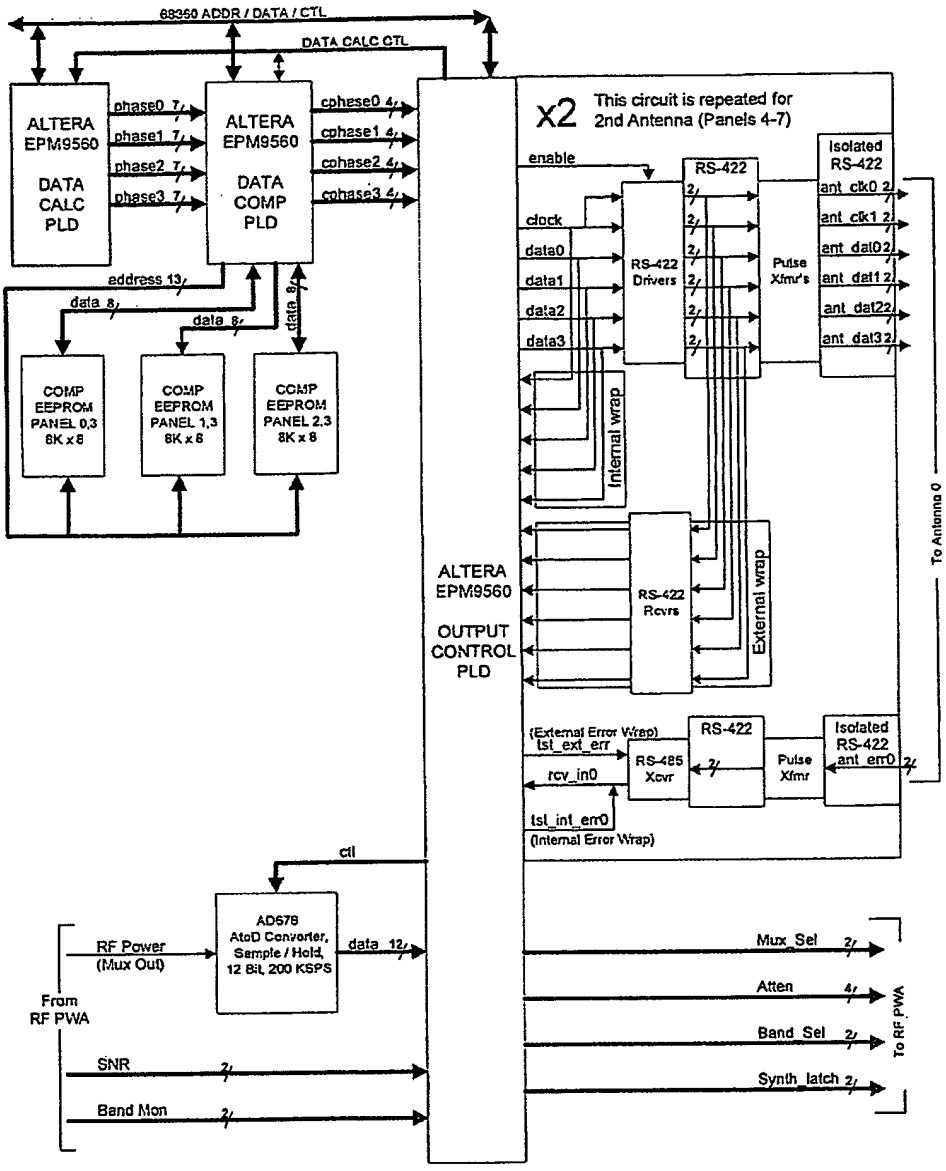


FIGURE 4.4-5. SPAC PHASE CALCULATION CIRCUIT BLOCK DIAGRAM

The EPLDs implement four identical computation channels and can generate phase shift data for up to four antenna panels simultaneously. The data calculator PLD computes phase data with 13 bit accuracy and passes 7 bits on to the data compensator. The compensator PLD adds a per element calibration constant and passes the data to the output controller. The output controller formats the phase data into messages which are then sent to the antenna. The output controller also controls the RF detector timing and on board A/D converter.

4.4.3.2 Data Calculator Hardware Algorithm (figure 4.4-6)

The Data Calculator EPLD computes individual phase shifter values for up to 8 subarrays. The

Data Calculator PLD contains 13 bit registers to hold the (qty 8) initial, (qty 1) delta, and (qty 2) flyback phase values that are computed and written by the host CPU. The 13 bit values are left justified to bit 14, in a 16 bit field. This allows S/W to assign a weight of 180° to bit 14, and allows bit 15 to act as an overflow bit (for angle calculations in S/W). The intent is to prevent S/W from having to do any shifting of the angle values, before writing them to the registers. Qty (4) 13 bit accumulators are used to hold a 13 bit phase shifter value. For each subarray, the accumulator is initially cleared. The 13 bit Initial Phase Register is added to the accumulator. The upper 7 bits of the accumulators, for each of the 4 panels, are then sent to the Data Compensator PLD, where they are then added to a 6 bit compensation value. The 6 bits of compensation data are connected to the upper 6 bits of the other adder input. Effective 6 bit rounding, from the 13 bit accumulator value to the 7 bit sum, from the compensation add, is accomplished by H/W setting the bit 0 of the compensation input to the 7 bit Compensation Adder. The result is then truncated to 4 bits. **Pre-rounding to the final 4 bit phase will be accomplished by external software adding 2H (11.25°) to each compensation value, before the data is written to the Antenna Compensation EEPROM's.** The final 4 bit result is sent to the output controller EPLD for formatting and output to the antenna. After generating the first 4 bit phase for the subarray, the Data Calculator PLD performs successive 13 bit sums of the Accumulator and the Delta Phase Register, storing the result in the Accumulator. Once 16 values have been generated, one of two Flyback Phase Registers are added to the accumulator to start the next data column.

Throughout the Data Calculator data path (registers, adders, and buses), the MSB is always 180°. This bit may also be thought-of as a sign bit. Any add which results in a carry-out from the 180° bit is equivalent to, *New_Angle* = Mod(*Angle*, 360°). When the 6 bit compensation value is measured / calculated on the external antenna calibration system, this representation (MSB = bit 5 = 180°) should be used for the 4 bit pre-round operation (adding 2H = 11.25°).

The Output Controller serializes the (4) 4-bit phase data streams and generates the control data (header, message type, subarray, column #, and parity), and then Manchester encodes the outputs. The second antenna (panels 4-7) phase data is generated using the same phase registers and data paths as for panels 0-3; therefore, the two antennas can not be loaded with phase data in parallel. Separate bank(s) of compensation data, for the second antenna, can be selected.

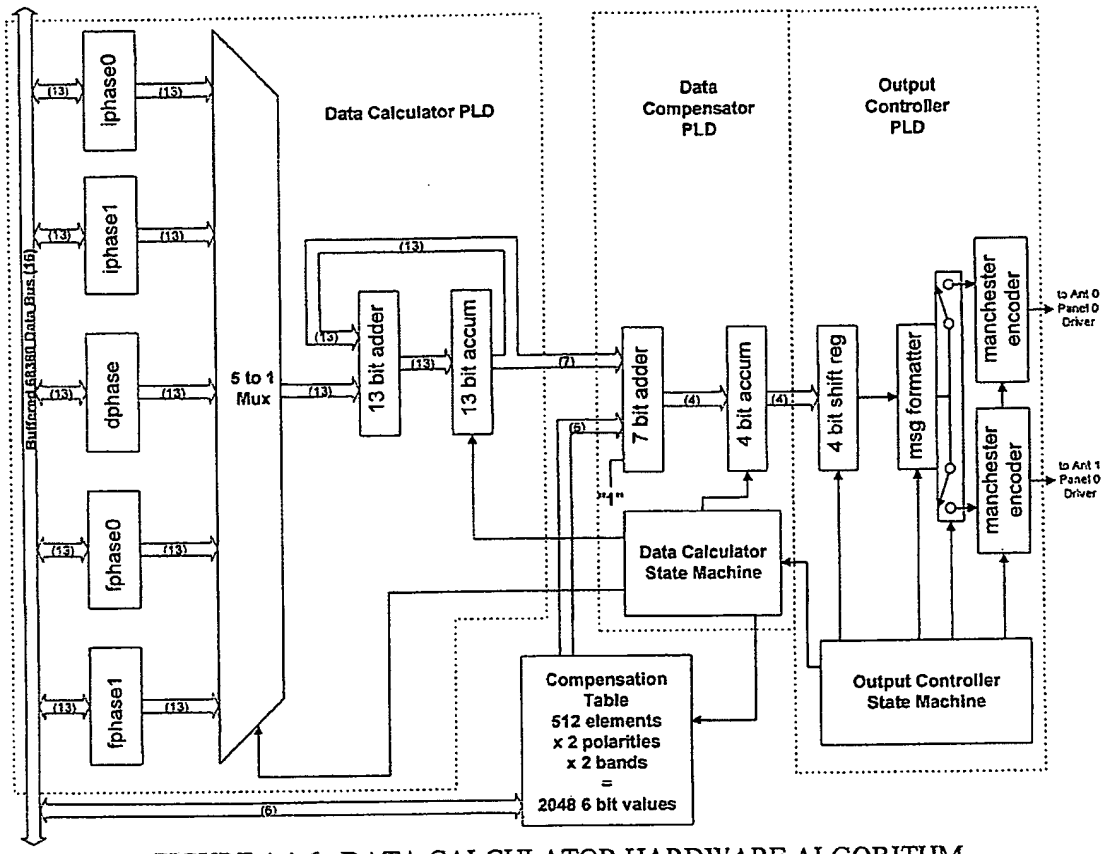


FIGURE 4.4-6. DATA CALCULATOR HARDWARE ALGORITHM

4.4.4 RF Card Description

The RF card contains the circuits necessary to measure the RF signals for each of two input channels (LHCP and RHCP) from the LNB. The RF card also provides band-control to the LNB. Figure 4.4-7 indicates the RF card block diagram. The RF Card is pictured in figure 4.4-8.

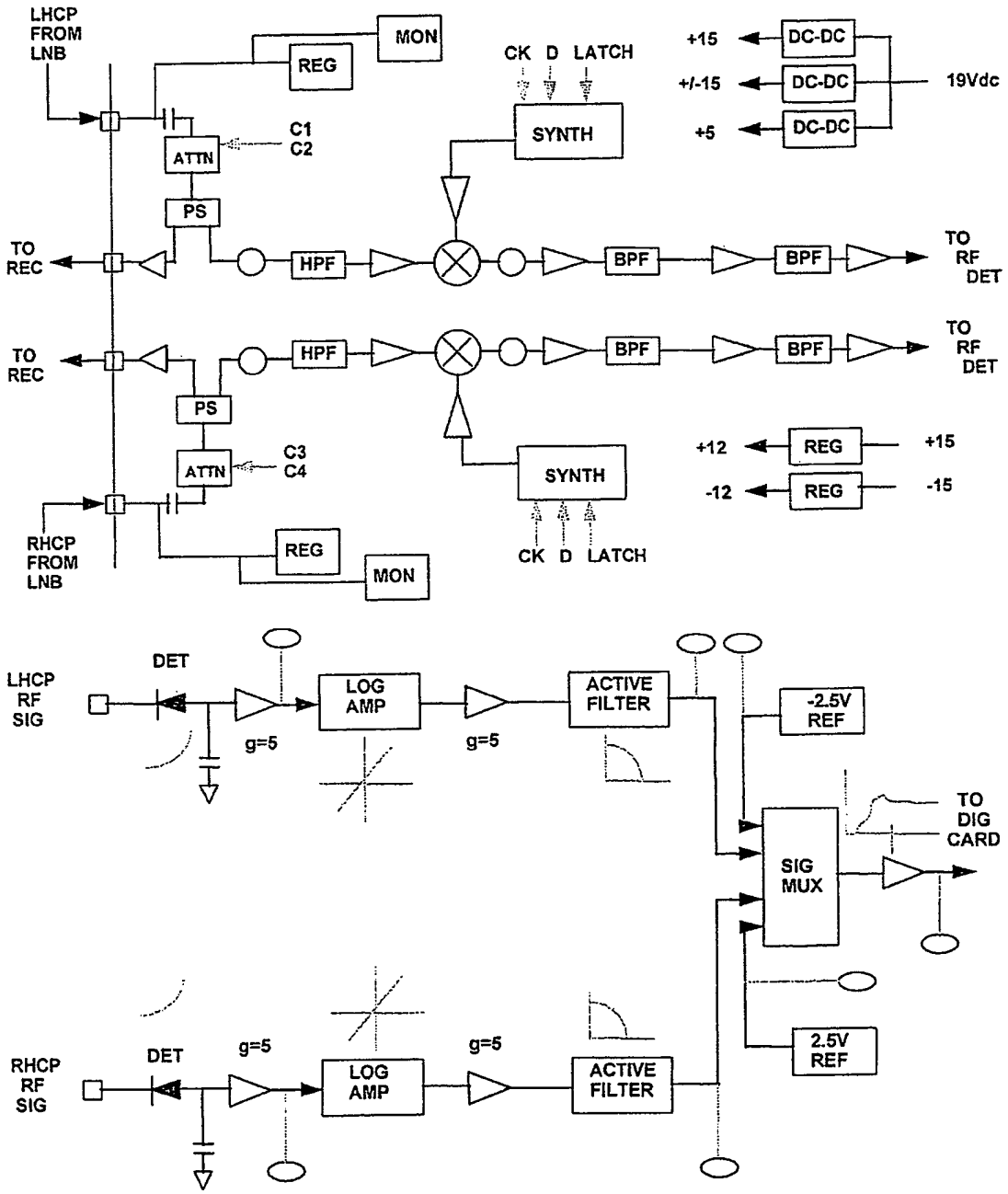


FIGURE 4.4-7. SPAC RF CARD BLOCK DIAGRAM

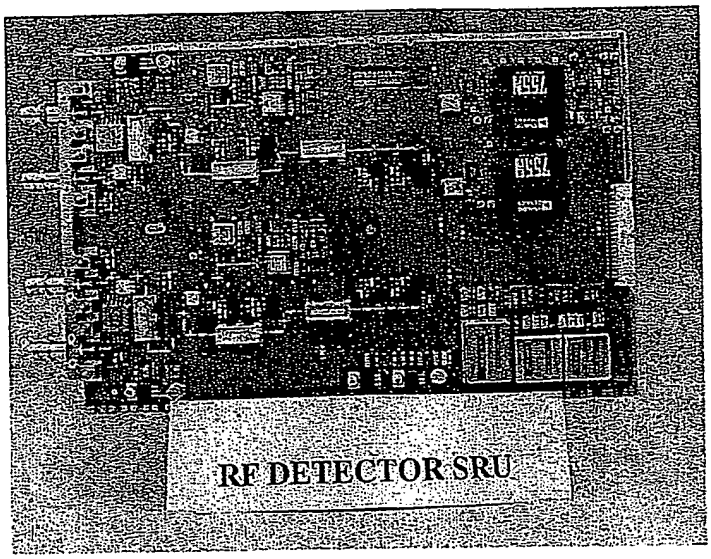


FIGURE 4.4-8. SPAC RF CARD

The RF card has the following allocated requirements within the SPAC:

- Measure relative signal levels for different beam positions.
- Relative accuracy over a one-second time interval signal power, single path < 0.05 dB.
- RF input signal-to-noise > 5 dB.
- Input dynamic range > 50 dB.
- Output dynamic range < 25 dB.
- A/D output resolution = 12 bit (+/- 4V DC = 0.006 dB)
- Beam position dwell time = 1.25 milliseconds.
- Selectable transponder for track control.
- Provide signal measurement for two independent channels.
- Supply DC bias voltage to dual LNB: 10-12V DC for Low-Band 11.7-12.2 GHz.
  13-15V DC for High-Band 12.2-12.7 GHz.

The RF card has the following design characteristics:

- Transponders on each polarization are individually selectable by a tunable local oscillator set by processor.
- Local oscillator synthesizer is phase-locked from 1400 to 1900 MHz.
- High-side local oscillator to minimize signal band interference.
- Detected voltages are logarithmically compressed to hold accuracy.
- Final video filtering by processor on 12-bit A/D samples.
- Programmable dynamic range attenuation 0-30 dB in 10-dB steps.
- Bessel active filters to form anti-alias filter prior to A/D.
- Independent dual channel RF detection capability.

In addition the RF card has the following EMI design provisions:

- Guard fence provisions (Faraday shield) for the synthesizers and DC-DC power converters.
- Lowpass filters between ground planes.
- Controlled-impedance layers 1-4, 50Ω ± 5Ω.
- Separated ground planes connected at chassis.
- No overlapping ground planes.
- Short RF path lengths.
- Microstrip RF signal paths.

4.4.5 Intercard Connector

The interface between the processor/data calculator and RF PWAs is a filter-pin connector on the RF shield. The connector allows the processor to read the A/D converter. A complete extension of the processor bus is not required between the two cards. The signals on the connector are listed in table 4.4-2.

TABLE 4.4-2. SPAC INTERCARD CONNECTOR SIGNALS

PIN	NAME	DESCRIPTION
1	Mux_sel(0)	Analog multiplexer select line
2	Mux_sel(1)	Analog multiplexer select line
3	d(0)	Digital data bit
4	d(1)	Digital data bit
5	d(2)	Digital data bit
6	d(3)	Digital data bit
7	d(4)	Digital data bit
8	d(5)	Digital data bit
9	d(6)	Digital data bit
10	d(7)	Digital data bit
11	d(8)	Digital data bit
12	d(9)	Digital data bit
13	d(10)	Digital data bit
14	d(11)	Digital data bit
15	convert	A/D conversion control bit
16	read	A/D read data control bit
17		
18-34	GND	Digital ground connections

4.4.6 External Connections

The SPAC supports the external interfaces indicated in figure 4.4-1 and table 4.4-3.

TABLE 4.4-3. SPAC EXTERNAL INTERFACE SIGNALS

Interface Name	Description	Type	Pins	Pin Names
Shop	Provides interface for software load, factory test, and shop diagnostics.	RS-232C	3	TXD, RXD, GND
Control/Status	Delivers remote status to an airplane system or display, and receives external mode and system control.	RS-232C	3	TXD, RXD, GND
Receiver Control Status	Digital interface to get receiver signal status and frequency selection.	RS-232C	3	TXD, RXD, GND
Receiver Video	Baseband video output to the receiver.	L-Band RF	Coax	Signal, Shield
IRU	Connection to the airplane inertial reference unit to aid in acquisition.	ARINC-429	3	
Power Supply	Voltage lines to power the SPAC	Discrete wires	6	+19.5V DC, 19.5Rtn
Power Status	Power supply fault detection and on/off control.	RS-485	4	Status1, Status2
LNB	Receive L-band RF from the LNB and provide band selection control to the LNB.	L-Band RF + DC	Coax	Signal, Shield
Antenna	Clock and data lines to/from the antenna. Used to control beam pointing (reference figure 4.1-13).	RS-422 differ-ential	12	Data0+ Data0- Data1+ Data1- Data2+ Data2- Clock0+ Clock0- Clock1+ Clock1- Error0+ Error0-

4.5 Antenna Switch Unit

The PACAS antenna switch unit (ASU) accepts the two single-polarization outputs from the SPAC (LHCP and RHCP), and provides up to 24 RF outputs (12 in each of two units) selectable as LHCP or RHCP to receivers. Power is provided from the receivers on ports #1, #5, and #9 via the polarization selection. The functional schematic for four channels is indicated in figure 4.5-1. An isometric drawing is displayed in figure 4.5-2 for a 12-channel unit.

The 12-channel unit is approximately 6" x 9" x 10" and weighs approximately 6.5 lbs (the 4-channel unit is 2.5" high and weighs 3.2 lbs.).

The ASU also provides switchable communications between the receivers and the SPAC (for signal validation and frequency control) in response to discrete input service selections (one receiver at a time). The ASU is considered to be an interim interface between the SPAC and receivers, primarily suitable for business jet or military VIP missions (few users, each with individual choice of channels).

The ASU has the following additional features:

- Up to 6 non-concurrent multiple services selectable (by connecting the RS-232 interface to the SPAC) using discrete inputs on one or two ASUs.
- Receivers 1, 2, 3,...24 access all programming from the current service.
- Up to 12 channels/ASU; maximum number of total receivers is 24.
- ASU power to each group of four ports can be received from any single receiver in the group (1-4, 5-8, 9-12, where power must be supplied to group 1-4 to enable operation of 5-8, and power must be supplied to groups 1-4 and 5-8 to enable operation of 9-12, power must be supplied to groups 1-4, 5-8, and 9-12 to enable operation of a second ASU. Power is supplied as 11-19V DC, ≤ 150 mA/receiver.

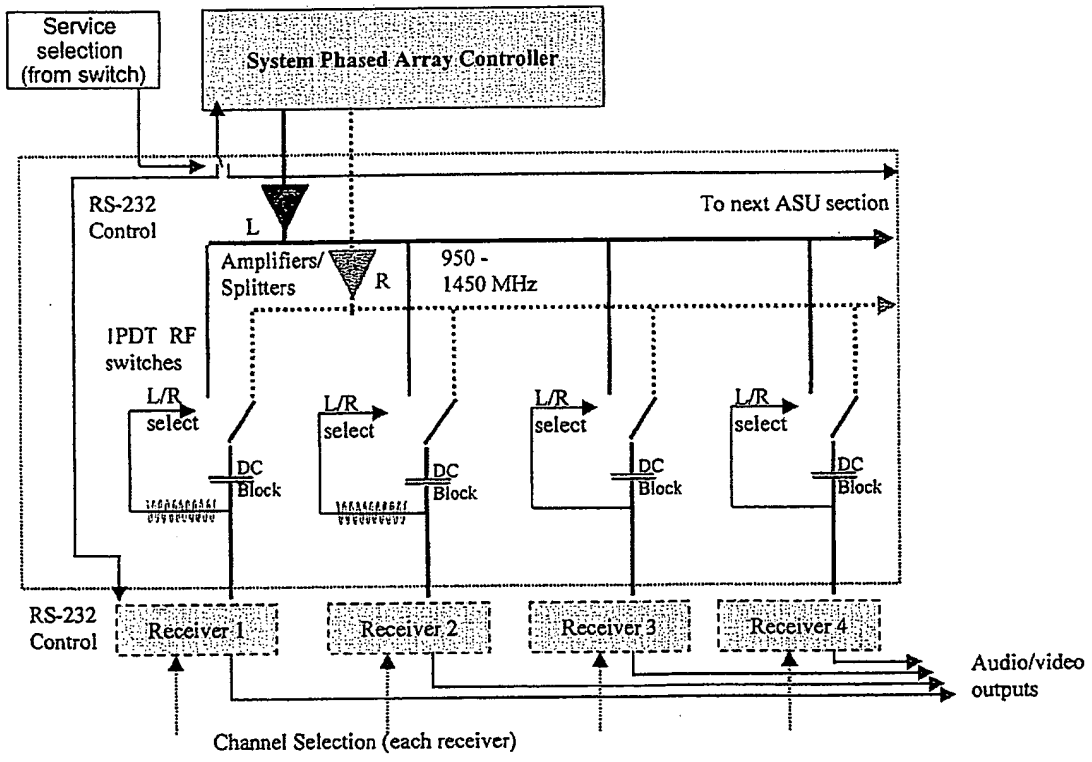


FIGURE 4.5-1 ANTENNA SWITCH UNIT CONTEXT/BLOCK DIAGRAM

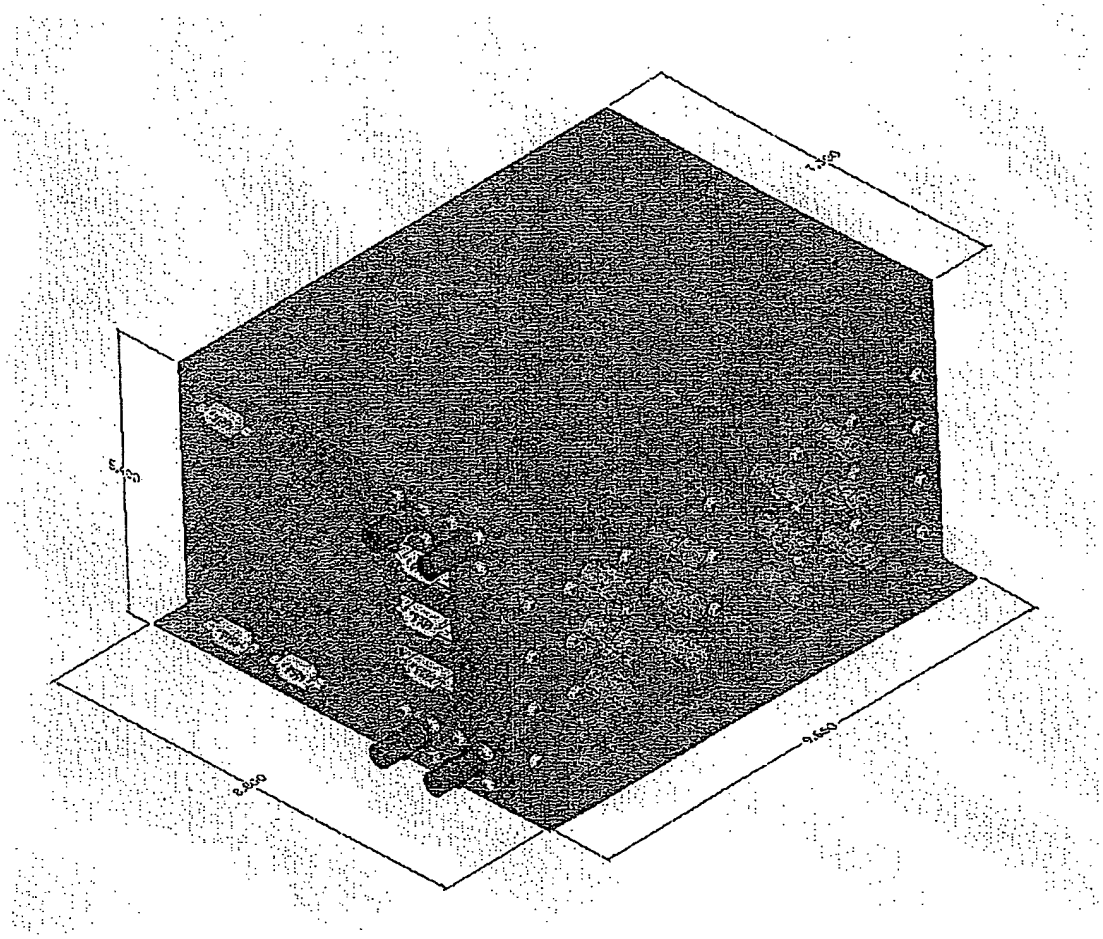


FIGURE 4.5-2 ANTENNA SWITCH UNIT ISOMETRIC DRAWING

4.6 COTS Receivers

The Commercial-Off-the-Shelf (COTS) receivers provide conversion of the input L-band RF into NTSC-compatible baseband video and associated audio. Inputs are channel selections, data requests, and L-band RF; outputs are audio and video analog, plus control signals back to the SPAC.

The control signals perform service selection by validating the required input, and selecting the transponder (frequency) and polarization associated with the selected channel. The polarization selection is accomplished as a DC level on the L-band RF input.

Input formats for decoding are the Hughes proprietary "DSS" (for Hughes DBS-1, -2, -3 satellites, with service from DirecTV and/or USSB), and MPEG2-DVB for the EchoStar/DISH network.

Output formats include "RCA" type jacks for the audio (stereo 1 kΩ, isolated, coax) and video (50Ω, isolated, coax) (additional video outputs are typically available but not baselined for use, *e.g.*, S-video, Channel 3/4).

Channel selection is via either the buttons on the front panel or using the supplied infrared (IR) or ultra-high frequency (UHF) remote. The control options are displayed on the connected television(s) for visual feedback to the operator ("on-screen programming").

Service is authorized by the "SmartCard" installed in the receiver. Service authorization requires that the service provider (DISH, DirecTV, USSB) receive the SmartCard and receiver serial numbers for recording in their operational database. The service provider transmits an authorization to the receiver (an indication of which programs may be decoded for the combination of SmartCard number and receiver serial number) on a periodic basis. The receiver retains the authorization, and verifies that the program selected by the operator is authorized prior to decoding and outputting the audio and video (reference section 3.3.5.1 for the ASU/COTS receiver operation).

Input power is 115V AC, 60 Hz. Receivers are FCC-approved and UL-listed. Environmental requirements are consistent with heated indoor, stationary, dry locations.

4.7 Cables

Interconnecting cables are identified in figure 4.7-1. Some installation flexibility is afforded using different-length cables between the LNB, SPAC, ASU, and receivers (reference STARS-PKG-CABL-023).

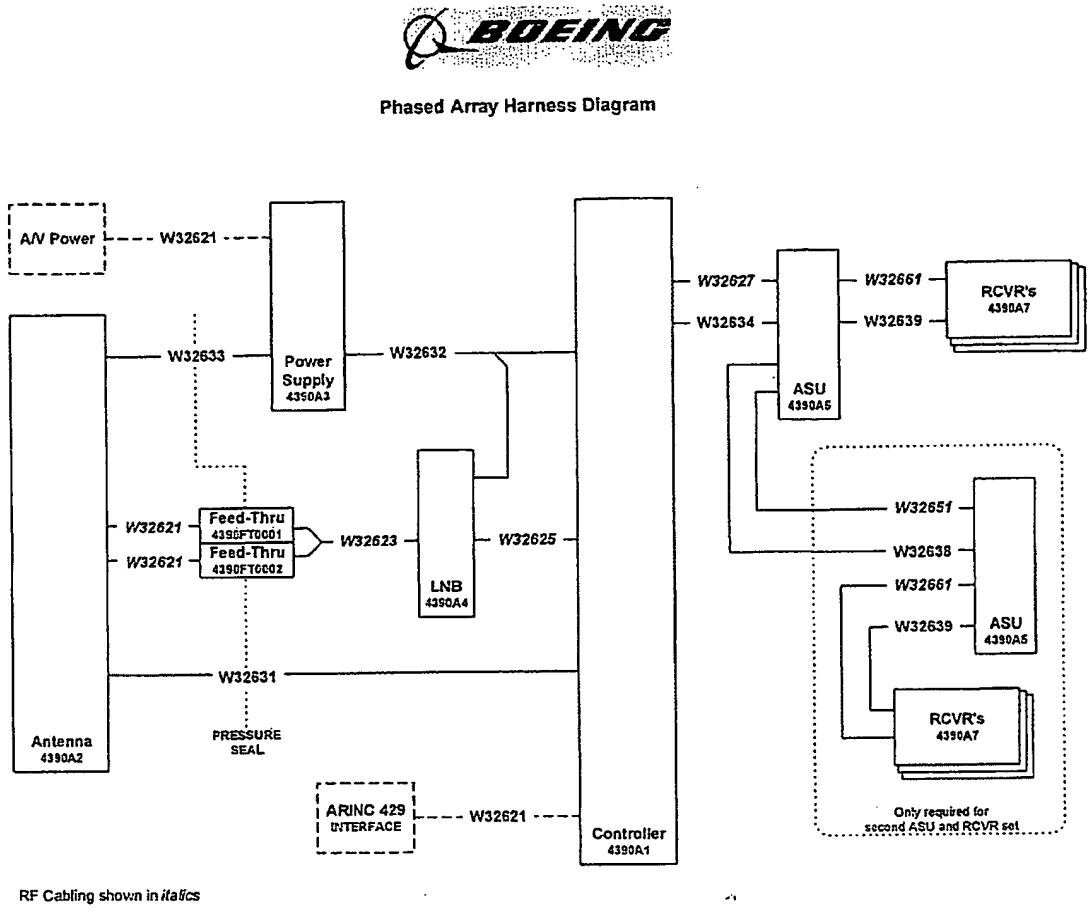


FIGURE 4.7-1 PACAS INTER-LRU CABLING

REVISIONS			
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